Trials@uspto.gov
571-272-7822

Paper 11
Entered: April 16, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HP INC., DELL TECHNOLOGIES INC., DELL INC.,
LENOVO (UNITED STATES) INC
Petitioner,

v.

UNIVERSAL CONNECTIVITY TECHNOLOGIES, INC.,
Patent Owner.

IPR2024-01429
Patent 7,187,307 B1

Before KARL D. EASTHOM, THOMAS L. GIANNETTI, and SHARON FENICK, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

HP Inc., Dell Technologies Inc., Dell Inc., and Lenovo (United States) Inc. (collectively) Petitioner, filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1, 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, and 75 (the "challenged claims") of U.S. Patent No. 7,187,307 B1 (Ex. 1001, the "'307 patent"). Pet. 1. Universal Connectivity Technologies Inc., Patent Owner, filed a Preliminary Response (Paper 8, "Prelim. Resp."). Patent Owner argues that we deny the Petition based on discretionary denial under 35 U.S.C. § 314. Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) ("[T]he PTO is permitted, but never compelled, to institute an IPR proceeding."). Because we agree with Patent Owner that we should discretionarily deny institution due to the state of parallel District Court litigation, and as explained more fully below, we do not institute *inter partes* review.

II. BACKGROUND

After the parties filed a respective Petition and Preliminary Response, the Office rescinded the June 2022 memorandum entitled "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation." Based on the change of binding guidance, we permitted additional briefing. Thus, Petitioner filed a Reply to the Preliminary Response ("Reply") (Paper 9) and Patent Owner filed a corresponding Sur-reply ("Sur-reply") (Paper 10) addressing discretionary denial.

A. Real Parties in Interest

Petitioner identifies Dell Inc., Dell Technologies Inc., HP Inc., Lenovo (United States) Inc., and Lenovo Group Ltd. as real parties in interest. Pet. 75. Patent Owner identifies itself as the real party in interest. Paper 6, 2.

B. Related Matters

Three parallel District Court cases involve the '307 patent (Paper 6):

1) *Universal Connectivity Technologies Inc. v. Dell Technologies Inc.*, *et al.*, No. 1:23-cv-01506-RP (W.D. Tex.) (the "Dell litigation");
2) *Universal Connectivity Technologies Inc. v. HP Inc.*, No. 4:24-cv-04097-YGR (N.D. Cal.) (the "HP litigation"); and
3) *Universal Connectivity Technologies Inc. v. Lenovo Group Limited*, No. 2:23-cv-00449-JRG (E.D. Tex.) (the "Lenovo Group litigation").

According to Patent Owner, there is a fourth case concerning a U.S. based, wholly-owned subsidiary of Lenovo Group, Lenovo US, and that action for declaratory judgment is pending in Delaware, No. 1:24-cv-01126-RGA. Prelim. Resp. 12 n.1. The parties do not raise any issues with this fourth litigation here.

Petitioner also identifies the following IPR proceedings as concurrent proceedings involving the same parties: IPR2024-01428, IPR2024-01478, IPR2024-01479, IPR2024-01480, IPR2024-01481, and IPR2024-01482. Pet. 75.

C. The '307 Patent

The '307 patent describes "[a] communication system including two endpoints (transceivers or a transmitter and receiver) and a serial link between them." Ex. 1001, code (57). One endpoint "generate[s] encoded data in accordance with a line code and to transmit the encoded data over the link." *Id.* "The line code specifies a block code for encoding cells of application data and control bits, and typically also special characters that do not match bit sequences of encoded cells." *Id.* Other aspects of the disclosed invention include "methods for performing functions of multiple layers of a communication protocol in response to such encoded data." *Id.* "In accordance with the invention, multiple levels of communication protocol functionality can be efficiently incorporated within a line code." *Id.*

D. Exemplary Claim 1

Claims 1, 23, 53, and 68 are independent. Independent claim 1 is illustrative of the challenged claims, and follows (with bracketed nomenclature by Petitioner):

> 1. [1(pre)] A communication system, including:
>
> [1.a] a first endpoint;
>
> [1.b] a second endpoint, including physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry; and
>
> [1.c] a serial link between the first endpoint and the second endpoint, [1.d] wherein the first endpoint is configured to generate encoded data in accordance with a line code, and to transmit the encoded data over the link to the second endpoint, and

[1.e] wherein the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data [1.f] to recover application data and control bits, [1.g] to perform at least one link level function in response to at least one of the control bits, and [1.h] to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry, and

[1.i] wherein the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

E. Asserted Grounds of Unpatentability

Petitioner contends that the challenged claims are unpatentable as follows:[1]

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 6, 7, 53	102 (a, e)	Shin[2]
1, 2, 6, 7, 53	103(a)	Shin
1, 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, 75	103(a)	Yusairi,[3] Shin

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102, 103 effective March 16, 2013, which is after the '307 patent's filing date. *See* Ex. 1001, code (22) (filed June 12, 2003). Therefore, the pre-AIA versions of §§ 102, 103 apply.

[2] Shin et al., US 2002/0159450 Al, published Oct. 31, 2002, filed Nov. 7, 2001. Ex. 1004.

[3] M. Yusairi, Bin Abu Hassan, Koki Abe, *Hardware Design and Implementation of IP-over-1394 Protocol Stack*, ITE Tech. Rep., V.27, No. 18, pp. 51–58 (Mar. 2003). Ex. 1005.

Pet. 8. Petitioner supports its Petition with a Declaration of Andrew Wolfe, Ph.D. Ex. 1003.

III. DISCRETIONARY DENIAL UNDER 35 U.S.C. § 314(a)

In exercising the Director's discretion under § 314(a), the Board may consider "events in other proceedings related to the same patent, either at the Office, in district court, or the ITC." Patent Trial and Appeal Board Consolidated Trial Practice Guide, 58 & n.2 (Nov. 2019) ("*CTPG*"). *NHK Spring* explains that the Board may consider the advanced state of a related district court proceeding, among other considerations, as a "factor that weighs in favor of denying the Petition under § 314(a)." *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential). Additionally, the Board's precedential order in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–16 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*") identifies several factors for analyzing issues related to the Director's discretion to deny institution in view of related litigation, with the goal of balancing efficiency, fairness, and patent quality.

When considering related litigation, the Board evaluates the following factors ("*Fintiv* factors"):

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;

3. investment in the parallel proceeding by the court and the parties;

4. overlap between issues raised in the petition and in the parallel proceeding;

5. whether the petitioner and the defendant in the parallel proceeding are the same party; and

6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv at 5–6.

A. Factor 1: whether the court granted a stay or evidence exists that one may be granted if this proceeding is institute

Of the three District Court proceedings, the Lenovo Group litigation, pending in the Eastern District of Texas, is the most significant to our analysis here. In the Lenovo Group litigation, the parties have not requested a stay. Prelim. Resp. 13. Patent Owner argues that the Lenovo Group litigation is not likely to be stayed based on that court's low grant rate in other cases and the progress of that case in particular. *Id.* at 13−16. The court in the HP litigation denied a stay without prejudice, and stated that a stay could be reconsidered in the future depending on the outcome at the PTAB. Reply 4. The Dell litigation has been stayed. *Id.*

On this record, we decline to speculate as to how any of the involved district courts where no stay is pending might rule on any future motion to stay. Thus, we determine that, while one stay has been granted, the lack of a stay in the other underlying District Court cases, especially the Lenovo Group litigation, is not sufficiently persuasive to weigh this factor against exercising discretion. Therefore, this factor has a neutral effect on the overall balancing of the *Fintiv* factors.

B. Factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

The scheduled trial date for the Lenovo Group litigation is November 3, 2025, which is about six months prior to the expected date for the final written decision here (i.e., late April 2026). *See* Prelim. Resp. 17; Ex. 2002 (Lenovo Group litigation Case Docket Control Order), 1 (listing trial date as Nov. 3, 2025). Petitioner argues this trial date is speculative. Reply 4. Further, Petitioner focuses its argument on what it terms a "growing backlog" in the Eastern District of Texas and the status of the HP litigation, which is currently set for trial on September 21, 2026. *Id.*

Patent Owner argues that "[b]oth the scheduled trial date and the date of trial based on median time-to-trial statistics occur many months before a final written decision would be expected here." Sur-reply 4. Patent Owner asserts that the time-to-trial statistics for the Eastern District of Texas project a median time-to-trial of 21.9 months. Prelim. Resp. 17–18. This projection yields a trial date of July 2025, which is about nine months prior to the expected final written decision date of April 2026. *See id.* at 18 (citing Ex. 2008 (U.S. District Courts—Federal Court Management Statistics–Profiles—September 30, 2024 Reporting)).

As with the previous factor, the status of the Lenovo Group litigation is our focus here. As stated, that trial is set to occur about six months before a final written decision would issue in this proceeding. The District Court has stated that this trial date setting "cannot be changed without an acceptable showing of good cause." Prelim. Resp. 17. We are not persuaded by Petitioner's unsupported argument that the trial date is speculative. We also consider the fact that the median time-to-trial statistic projects a trial date of July 2025, earlier than the actual date set by the

District Court. Ex. 2002; Ex. 2008; Prelim. Resp. 17–18. The fact that the time-to-trial statistic is earlier than the trial date set by Judge Gilstrap confirms that the schedule set by the District Court is credible and should be given weight. From this evidence, we are persuaded that we should rely on the trial date in the Lenovo Group litigation as the main indicator of a trial court reaching the merits of the invalidity of the patent-at-issue before we issue a final written decision.

Accordingly, this factor strongly favors exercising discretionary denial.

C. Factor 3: investment in the parallel proceeding by the court and the parties;

This factor relates to the "amount and type of work already completed in the parallel litigation by the court and the parties at the time of the institution decision." *Fintiv* at 9.

As for the amount and type of work expended by the parties, we understand that Patent Owner has "conducted extensive third-party discovery from [Lenovo Group Limited]'s suppliers." Prelim. Resp. 19. By the time the institution decisions issue, the parties would have completed the claim construction briefing, with a *Markman* hearing scheduled soon, i.e. for May 20, 2025. *See id.*; Sur-reply 3.[4] This activity is all in connection with the Lenovo Group litigation; the Dell and HP litigations have had no significant activity of note. Reply 5. As for the District Court's work in the Lenovo Group litigation, although there have been discovery motions and

[4] The District Court recently re-scheduled the *Markman* hearing to May 20, 2025, from its originally scheduled date of May 12, 2025.

other activity in connection with claim construction, the amount of work that has been performed to date does not support a concern for the investments made in that litigation.[5]

Balancing the evidence before us, we are persuaded that the Lenovo Group litigation activity by the court and the parties has little to no impact on the analysis of the third factor. Accordingly, this factor is neutral.

D. Factor 4: overlap between issues raised in the petition and in the parallel proceeding;

Under the fourth *Fintiv* factor, we consider "overlap between issues raised in the petition and in the parallel proceeding." *Fintiv* at 12. Petitioner stipulates that if we institute trial, Petitioner "will not to pursue in District Court litigation the specific grounds asserted in *inter partes review* [], or on any other ground that was raised or could have been reasonably raised in an IPR." Ex. 1017 (stipulation by Dell Technologies Inc., and Dell Inc., and citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential)); Ex. 1018 (identical stipulation by HP Inc.); Ex. 1019 (identical stipulation by Lenovo (United States) Inc.); Ex. 1020 (identical stipulation by Lenovo Group Limited).

In its Sur-reply, Patent Owner contends that the *Sotera* stipulations do not mitigate concerns of overlap because the stipulations state that Petitioner "expressly reserved the right to challenge invalidity at the district court based on the same references relied upon here in combination with 'any system, product, or public knowledge or use that embodies' any of the identified prior art patents or printed publications." *See* Sur-reply 5 (quoting

[5] As noted *supra*, a *Markman* hearing has not been held, and thus, to date, there is no *Markman* order that would require efforts by the District Court.

Ex. 2005, 29; citing Ex. 1028, 2 n.1). We do not agree with Patent Owner. The overlap of claims between this proceeding and the litigation is complete, and the prior art references involved here are the same as some of the prior art involved in the litigation. Prelim. Resp. 20–21. Although we acknowledge Patent Owner's concern about lack of overlap stemming from Petitioner's reservation of rights in its *Sotera* stipulation, our evaluation at this juncture is based on the facts before us, not on how Petitioner *might* challenge the validity of the patent at trial. Further, Patent Owner does not identify any art asserted by Petitioner in the litigation that might fall within this reservation. On the present record, Petitioner's broad stipulation mitigates certain concerns of duplicative efforts between the District Court and the Board, and also concerns of potentially conflicting decisions. *Sotera*, Paper 12 at 19.

Accordingly, factor 4 strongly favors not exercising discretionary denial.

E. Factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party;

Under the fifth *Fintiv* factor, we consider "whether the petitioner and the defendant in the parallel proceeding are the same party." *Fintiv* at 13. "[I]f the parties are the same in the *inter partes* proceeding and in the parallel proceeding. . . . this factor supports denying institution." *Sotera* at 19 (citations omitted). Patent Owner states that "there is no dispute that Petitioners are defendants" in the Lenovo Group litigation, and the Dell litigation and the HP litigation are the same in that respect. Prelim. Resp. 22.

Petitioner contends that Factor 5 "is, at worst, neutral." Reply 5. Petitioner contends that "*Fintiv* did not suggest Factor 5 favors denial when the petitioner is the defendant." *Id.* (citing *Fintiv* at 13–14). Petitioner notes that "neither Dell nor HP is a party" in the Lenovo Group litigation, upon which Patent Owner relies, and the fact "that Dell and HP are parties to [the Dell litigation and the HP litigation] has no bearing on Factor 5." *Id.*

Patent Owner contends that "[b]ecause the [P]etitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial." Prelim. Resp. 22.

On the record before us, we discern no reason to treat Petitioner Lenovo (US) and its parent as separate parties for the purpose of this *Fintiv* analysis. Petitioner identifies Lenovo Group Limited as a real party in interest. Pet. 75 ("Petitioners hereby name Dell Inc., Dell Technologies Inc., HP Inc., and Lenovo (United States) Inc. as real parties-in-interest and, solely because it is named as a defendant in a co-pending District Court case listed below, further identify Lenovo Group Ltd. as a real party-in-interest."). Lenovo Group Limited has submitted a *Sotera* stipulation in this case. Therefore, all the parties comprising Petitioner are involved as defendants or as a real party-in-interest to a defendant in the parallel District Court litigations.

Accordingly, factor 5 weighs in favor of discretionary denial.

F. Factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

This sixth factor takes into account other circumstances that may bear on the decision to exercise discretion to deny, such as the merits of the patentability challenges. *Fintiv* at 14–16. This factor also supports the

exercise of discretion because on the merits of the case, on the present record, there are weaknesses that call into question the strength of the Petition. *See Fintiv* at 15 ("[I]f the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present. . . there may be strengths or weaknesses regarding the merits that the Board considers as part of its balanced assessment"). We therefore turn to a discussion of the merits.

1. Level of Ordinary Skill

The person of ordinary skill in the art is a hypothetical person who knows the relevant art. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors in determining the level of ordinary skill in the art include the types of problems encountered in the art, the sophistication of the technology, and educational level of active workers in the field. *Id.* One or more factors may predominate. *Id.*

Relying on its declarant, Dr. William H. Mangione-Smith, Patent Owner contends that

> [a] person of ordinary skill in the art of the subject matter of the '307 patent would have the equivalent of a bachelor's degree in electrical engineering, computer engineering, computer science, or equivalent training and three years of work experience with data communications systems or interfaces, including at least some experience with serial or display data communications

> systems or interfaces. . . . Additional education may compensate for lesser work experience, and vice versa.

Prelim. Resp. 6 (citing Ex. 2001 ¶ 15). Relying on its declarant, Dr. Wolfe, Petitioner proposes materially the same level. Pet. 5 (citing Ex. 1003 ¶¶ 26–29).

Based on a review of the record, we adopt the parties' proposed level of ordinary skill in the art because it is consistent with the evidence of record, including the asserted prior art and '307 patent.

2. Claim Construction

In *inter partes* reviews, the Board interprets claim language using the same standard used in district courts, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2023). Under this standard, claim terms have their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1313–14.

Petitioner contends that "wherein the first endpoint is configured to generate encoded data in accordance with a line code" in limitation 1.d and "wherein the . . . circuitry of the second endpoint configured to decode the encoded data [1.f] to recover application data and control bits" in limitation 1.e do not require the first endpoint to encode application data and control bits or, at least, do not require the first endpoint to encode application data and control bits together. *See* Reply 1–2. Petitioner explains that "while these claims also recite 'decod[ing] the encoded data to recover application and control bits,' they do not specify that ***both*** application data and control

bits must have been ***encoded***, much less whether both must have been encoded ***together***, to allow for their recited recovery."

Petitioner is correct to the extent that claim 1 specifies that "the first endpoint is configured to generate encoded data" without explicitly mentioning encoding any application data or control bits. However, this does not end the inquiry.

Disagreeing with Petitioner's claim construction, Patent Owner contends that "'encoded data' must include both application data bits and control bits." Sur-reply 1. According to Patent Owner, the specification confirms "[t]he plain and ordinary meaning of 'encoded data.'" *Id.* Patent Owner relies on the following passage of the specification:

> Another aspect of the invention is an endpoint device . . . configured to generate ***encoded data*** in accordance with a line code (where the line code specifies a block code ***for encoding cells of application data and control bits***, and typically also specifies special characters that are distinguishable from bits of encoded cells)[.]

Sur-reply 1 (emphasis and alterations in original) (quoting Ex. 1001, 8:47–55).

The parties each raise facially valid points based on the claim language. Petitioner has the burden to show "[h]ow the challenged claim is to be construed." 37 C.F.R. § 42.104 b(3). Petitioner does not explain how, under its broad construction, the decoder "decodes the encoded data t*o recover application and control bits in accordance with a line code*." That is, if the encoding does not encode both "application and control bits," then how can decoding "recover" both under Petitioner's claim construction? It is not clear on this preliminary record whether the specification supports Petitioner's broad claim construction.

For this reason, Petitioner's showing based upon the broad claim construction outlined above is not "particularly strong." *See Fintiv* at 14–15. As discussed further below, Petitioner also presents a showing under Patent Owner's more narrow construction.

3. Grounds 1 and 2, Alleged Anticipation or Obviousness of Claims 1, 2, 6, 7, and 53 Based on Shin

Petitioner contends that Shin anticipates or would have rendered obvious claims 1, 2, 6, 7, and 53. Pet. 11–37. Patent Owner disagrees. Prelim. Resp. 24–35.

a) Shin (Ex. 1004)

Shin relates to "a serial data communications architecture for communication between hosts and data store devices." Ex. 1004, code (57). The architecture provides "packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information." *Id.*

The "architecture may . . . specify encoding techniques to optimize transitions and to ensure DC-balance." Ex. 1004 ¶ 71. "Also, when a synchronization primitive encodes the packet type, then the link layer, rather than the transport layer, can detect packet type, which can enhance the overall processing speed." *Id.* ¶ 71.

b) Analysis of Claim 1

(1) Limitations 1.c–1f

Limitations 1.c and 1.d recite "[1.c] a serial link between the first endpoint and the second endpoint," and "[1.d] wherein the first endpoint is configured to generate encoded data in accordance with a line code, and to transmit the encoded data over the link to the second endpoint." For

limitation 1.c, Petitioner reads the recited "serial link" onto Shin's links 140 in Figure 1. Pet. 14–15 (citing Ex. 1004, Fig. 1, ¶ 75 (disclosing host and endpoints "are interconnected to switching network 130 via serial communication links 140")).

For limitation 1.d, Petitioner contends that

> Shin discloses using 8B/9B block encoding to encode 8-bit data into 9-bit symbols (i.e., into a larger number of bits), Ex.1004 at [0131], and transmitting them to "optimize transition control," maintain clock recovery and error detection, and "ensure DC-balance." *Id.*, Abstract, [0071], [0077], [0123]–[0124], [0128]; Ex.1003, ¶72–74. As such, a POSITA would have understood the Shin encodes data *in accordance with a line code*. Ex.1003, ¶75.

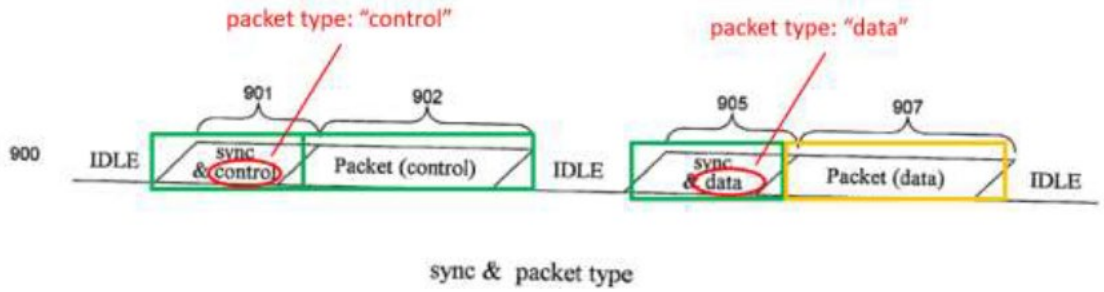
Pet. 16.

Petitioner also contends that "Shin discloses an example of a line encoding technique in another way." Pet. 16. That is, Petitioner contends that "Shin teaches using selective block inversion to transition optimize a block code." *Id.* (citing Ex.1004 ¶¶ 131–132 ("The encoding technique may also help ensure DC-balance by using selective block inversion encoding on symbols that have been transition optimized"). Based on these teachings, Petitioner contends that a "POSITA would have understood that selectively inverting encoded symbols to generate DC-balance requires a line code." *Id.* (citing Ex. 1004 ¶¶ 132; Ex.1003 ¶ 75). Petitioner explains that "Shin's host transmitter (*the first endpoint*) *is configured to generate encoded data in accordance with a line code* (at least by selectively inverting 9-bit symbols), *and to transmit the encoded data* (the selectively inverted symbols) *over the link* (the serial communication link) *to the second endpoint* (the data store device)." *Id.* at 16–17 (citing Ex.1003 ¶ 75).

As discussed further in connection with limitations 1.e and 1f below, Petitioner also contends that Shin's "host . . . transmits primitives, such as synchronization primitives that encode packet type, which may be transmitted immediately prior to packets to designate their packet type." Pet. 17–18 (citing Ex. 1004 ¶ 97, Fig. 9A).

Limitations 1.e and 1.f recite "[1.e] wherein the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data [1.f] to recover application data and control bits."

Petitioner relies on its the annotated version of Shin's Figure 9A, which follows:



According to Petitioner, Figure 9A above shows "synchronization primitive 901 encoded with a packet type of 'control' . . . transmitted immediately prior to a control packet 902, and a synchronization primitive 905 encoded with a packet type of 'data' . . . transmitted immediately prior to a data packet 907." Pet. 17–18 (citing Ex.1003 ¶¶ 79–80, 97).

Patent Owner argues that "Shin does not disclose encoding both application data bits and controls bits to create 'encoded data' that is decoded to recover both application data bits and controls bits. Petitioner[] rel[ies] on Shin's disclosure of primitives as the recited 'control bits' of the claims." Prelim. Resp. 24. Patent Owner explains that "[t]he primitives in

Shin . . . are not and cannot be the recited control bits of independent claims 1 and 53 at least because they are never encoded prior to transmission and they are never decoded upon receipt." *Id.* This line of argument relates to Patent Owner's narrow claim construction, where Petitioner's broad claim construction is not particularly strong on this preliminary record for the reasons noted above.

With further respect to the narrow claim construction, as summarized above, it is not clear if Petitioner relies on Shin's primitives (control bits) in addition to decoding application data. *See* Pet. 18–20 (citing Ex. 1004 ¶¶ 77, 96–98, 111–115, 146, 163, 165, 168, 170–171, Figs. 9C, 13; Ex. 1003 ¶¶ 79–85, 87–88). Petitioner cites Shin as disclosing that decision blocks in "the component decodes the primitive." *Id.* at 19 (citing Ex. 1004 ¶ 146). However, Petitioner appears to rely on what it refers to as a "line code" to reach the narrow construction and not on encoding application data and parsing primitives. *See id.* at 20.

To the extent Petitioner relies on parsing primitives with or without an additional line code, Petitioner does not adequately explain how primitives represent "encoded data in accordance with a line code" as claimed. Primitives appear to represent a symbol or number that Shin's process uses to represent that symbol in optimal binary form. *See* Ex. 1004 ¶¶ 99–101, Table 1 (showing primitives as binary representations of numbers as codes). However, as indicated above, it is not clear if Petitioner relies on primitives as part of the claimed line code. *See* Pet. 15–17 (relying on block encoding techniques as a line code without discussing primitives); Pet. 20. For these reasons, on this preliminary record, Petitioner's reliance on primitives is not particularly strong.

As indicated above, Petitioner also contends that Shin discloses a line code in the form of an encoding process that results in DC-balance. Pet. 15 (citing Ex. 1004 ¶ 128; Ex. 1003 ¶¶ 70–71). Petitioner alternatively relies on a similar type of line code that also results in DC-balance, namely Shin's selective block inversion technique to optimize a block code. *Id.* at 16 (citing Ex. 1004 ¶¶ 131–132). In both instances, however, Petitioner does not clearly show or allege that Shin's block codes apply to Shin's control data. *See* Pet. 15–17, 20. With respect to decoding, Petitioner states that a person of ordinary skill would have understood that primitives "are recovered from the line code." *Id.* at 20 (citing Ex. 1003 ¶¶ 87–88). Even if, by "line code," Petitioner refers to the two block encoding processes discussed above (which result in DC-balance), it is not clear on this preliminary record that Shin applies those encoding processes to Shin's primitives. *See* Ex. 1004, Fig. 9C (disclosing separate data encoder and control primitive generator); Pet. 19 (relying on same).

Based on the foregoing discussion, the preliminary record as summarized above is not "particularly strong" as to limitations 1.e and 1.f.

(2) Summary of Claim 1

Based on the analysis set forth above, including the analysis of Patent Owner's arguments and evidence, we determine on the current record that Petitioner's allegations of anticipation by Shin and obviousness over Shin are not particularly strong as to claim 1.

c) Analysis of Claims 2, 6, 7, and 53

Claims 2, 6, and 7 depend directly or indirectly from independent claim 1. For preliminary purposes, independent claim 53 is materially similar to independent claim 1. Petitioner relies on its showing for claim 1

to address claim 53, and contends that Shin anticipates or would have rendered obvious dependent claims 2, 6, and 7. Pet. 27–37. Patent Owner relies on its arguments for claim 1 to address dependent claims 2, 6, and 7, and relies on similar arguments to address independent claim 53. Prelim. Resp. 28–36. For reasons similar to those discussed above in connection with claim 1, Petitioner's allegations of anticipation by Shin and obviousness over Shin for claims 2, 6, 7 and 53 are not particularly strong.

4. Ground III, Alleged Obviousness of Claims 1, 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, and 75 Based on Yusairi and Shin

Petitioner contends that the combination of Yusairi and Shin would have rendered claims 1, 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, and 75 obvious. Pet. 37–74. Patent Owner disagrees. Prelim. Resp. 36–51.

a) Yusairi (Ex. 1005)

Yusairi generally relates to transmitting packets for applications over a home computer network devices using a protocol stack on a subset of the Internet protocol IP over IEEE1394 interface (IP over 1394). Ex. 1005, Abstract. Each device includes a physical layer, link layer, transport layer, and a higher-level network layers. *Id.* at 53–54.

b) Analysis of Claim 1

(1) Limitations 1.c–1f

Limitations 1.c and 1.d recite "[1.c] a serial link between the first endpoint and the second endpoint, [1.d] wherein the first endpoint is configured to generate encoded data in accordance with a line code, and to transmit the encoded data over the link to the second endpoint, and."

Petitioner reads the recited "serial link" of limitation 1.c onto Shin's IEEE1394 cable in Figure 6. Pet. 42 (citing Ex. 1005, 56 § 7.11, Fig. 6). For limitation 1.d, Petitioner contends that Yusairi discloses generating

encoded data in accordance with a line code because SOPC Board A encapsulates packets and transmits them to SOPC Board A, which decapsulates them. *Id.* at 43 (citing Ex. 1005. 56 § 7.1.2; Ex. 1003 ¶¶ 151–152). Petitioner alternatively contends that Yusairi employs IEEE1394, which uses an NRZ line code. *Id.* at 43–44 (citing Ex. 1005, 56 § 7.1.1 (disclosing that the SOPC Boards employ an IEEE1394 chip); Ex. 1008, 15, 81–82, 95 (disclosing that IEEE1394 employs an NRZ line code to communicate over a bus)).

Limitations 1.e and 1.f recite "[1.e] wherein the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data [1.f] to recover application data and control bits."

For limitation 1.e, Petitioner contends that Yusairi's Figure 6 shows that the second endpoint, SOPC Board B, receives and decodes packets from SOPC Board A over the IEEE1394 cable. Pet. 44 (citing 1005, 56 § 7.1.1, Fig. 6; Ex. 1003 ¶¶ 154–155). Petitioner further explains that "at SOPC Board A, packets are 'encapsulated and transmitted to the SOPC Board B,'" and "[a]t SOPC Board B, '[r]eceived packets [are] decapsulated.'" *Id.* at 45. (last two alterations in original) (quoting Ex. 1005, 56 § 7.1.2). Petitioner relies on the IEEE1394 standard to show decoding using an NRZ line code. *Id.* at 43 (citing Ex. 1005, 56, Sec. 7.1.1); Reply 3.

For limitation 1.f, Petitioner contends that "[a]t SOPC Board A (the first endpoint), the stream_trans module 'generates a link header, [and] attaches it to IP data.'" Pet. 46 (alteration in original) (quoting Ex.1005, 54 § 5.2). Petitioner contends that the link header includes "a transaction code" and "a type field" therein, which are "control bits," as claimed. *Id.* (citing

Ex. 1005, 54–55 § 5.2). Petitioner explains that SOPC Board A "transmit[s] [the link header and IP data packet] to SOPC Board B [*the second endpoint*]." *Id.* (last alteration in original) (quoting Ex. 1005 56, Sec. 7.1.2; citing Ex.1003 ¶¶ 160–161).

Petitioner refers to its explanation in connection with limitation 1.e, above, and contends that Yusairi's physical and link layers at SOPC B decode the received packets, which "recover" the control bits as limitation 1.f requires. Pet. 47. According further to Petitioner,

> [a] POSITA would have understood that the *control bits* of the transaction code and type field are "recovered" because the link layer uses them to determine the value of the transaction code "to start the header check process" and the value of the type field to assert a "ready signal" to the network layer.

Id. (citing Ex. 1005, 54–55 §§ 5.2–5.2; Ex. 1003 ¶ 163). Petitioner also contends that Yusairi's physical and link layers recover application data as claimed, because Yusairi recovers IP data in the packet by decoding it so that it can be "accepted and handed to the ip_rec [module of the network layer]." *Id.* at 48 (citing Ex. 1005, 55 § 5.2; Ex.1003 ¶ 164 (testifying that Yusairi's IP data is application data, which the physical and link layers recover, so that the data is accepted and handed to the network layer)).

Patent Owner contends that "[l]ike Shin, Yusairi fails to disclose encoding both application data bits and control bits to create encoded data for transmission and fails to disclose decoding the encoded data to recover application data bits and controls bits." Prelim. Resp. 36. Addressing Petitioner's reliance on the alleged NRZ line code, Patent Owner argues that "Petitioners have not explained how the 'transaction code' and 'type field values could be encoded without causing them to change format and be ignored." *Id.* at 42. In particular, Patent Owner argues that "Petitioner[]

ha[s] not shown that the 'transaction code' and 'type field' values in the link header are the recited 'control bits' of the claim at least because Yusairi indicates that those values are to remain as whole values and therefore, would not be encoded." *Id.* at 41 (arguing that "[a]ccording to Yusairi, the 'transaction code' and the 'type fi[el]d' values are checked as whole values (0xA and 0x0080 respectively) (citing Ex. 1005 § 5.2);" *see also* Sur-reply 3 ("This is problematic because those pre-fixed values in Yusairi are checked as whole, and if they are divided into individual bits or if bits are added, their values change, and the datagram would be ignored or discarded.")).

Petitioner replies that "[t]his argument relies on the same incorrect construction and is also tellingly unsupported by its declarant." Reply 3 (citing Prelim. Resp. 41–42). Petitioner's Reply does not address Patent Owner's specific argument in relation to the narrow claim construction and instead appears to rely on Petitioner's broad claim construction (which is not "particularly strong" as determined above). *See id.* Although, as Petitioner argues, Patent Owner does not rely on a declarant, Patent Owner reasonably supports its argument by citations to Shin as summarized above, raising a colorable issue on this preliminary record in light of Petitioner's Reply. Therefore, on this preliminary record, Petitioner's reliance on the NRZ code in Yusairi is not "particularly strong." *See Fintiv* at 14–15.

Petitioner's reliance on encapsulation as a form of encoding is also not particularly strong. Patent Owner argues that "[e]ncapsulation does not change the underlying bits in anyway; instead, encapsulation merely repackages the data." Prelim. Resp. 39 (Ex. 2001 ¶ 35). Patent Owner also argues that "by Petitioners' own dictionary definitions, encapsulation, as described in Yusairi, is not encoding as described in the '307 [p]atent." Sur-

reply 2. Patent Owner's arguments raise a valid point. Petitioner's showing is not particularly strong because it appears that packet encapsulation, a term of art, is distinct from encoding, another term of art. *See* Prelim. Resp. 39 (citing Ex. 1023 (encapsulation), 40 (citing Ex. 1020 (8b/10b encoding)). Petitioner does not point to a disclosure in the specification that supports reading such an overlap of two distinct terms of art.

In summary, Petitioner's showing based on Yusairi is not particularly strong.

(2) Summary of Claim 1

Based on the analysis set forth above, including the analysis of Patent Owner's arguments and evidence, we determine on the current record that Petitioner's allegation of obviousness over Yusairi and Shin is not particularly strong as to claim 1.

c) Analysis of Claims 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, and 75

Claims 2, 6, and 7 depend directly or indirectly from claim 1. Claims 23, 53, and 68 are independent. Claims 25 and 31 depend directly from claim 23. Claims 70–72, 74, and 75 depend directly or indirectly from claim 68.

For purposes of analysis at this preliminary stage, independent claim 53 is materially similar to independent claim 1. Petitioner relies on its showing for claim 1 to address claim 53, and contends that the combination of Yusairi and Shin would have rendered obvious dependent claims 2, 6, 7, 25, 23, 31, 53, 68, 70–72, 74, and 75. Pet. 50–74.

Patent Owner relies on its arguments for claim 1 to address independent claim 53. Prelim. Resp. 37–43. For reasons similar to those in connection with claim 1, Petitioner's showing for claim 53 based on

obviousness over Yusairi and Shin is not particularly strong. *See* Pet. 50–74.

Claim 23 recites the following (with bracketed nomenclature by Petitioner):

> [23.pre] A communication system, including:
> [23.a] a first endpoint;
> [23.b] a second endpoint; and
> [23.c] a serial link between the first endpoint and the second endpoint,
> [23.d] wherein the first endpoint is configured to encode M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where N>M,
> [23.e] the code word sequence is indicative of at least one cell of the input words, the input words of each said cell are indicative of application data and control bits,
> [23.f] the control bits have multiple levels of communication protocol functionality, and
> [23.g] the first endpoint is configured to transmit encoded data including the code words of the code word sequence over the link to the second endpoint.

Petitioner relies on its analysis of claim 1 to address claim 23's preamble and limitations 23.a–23.c. Pet. 53–54. Petitioner relies on the combination of Yusairi and Shin to address limitations 23.d, 23.e, and 23.g, and relies on Yusairi to address limitation 23.f, referring to its analysis of claims 2 and 6, which recite similar limitations. *Id.* at 54–56. Patent Owner presents similar arguments with respect to independent claim 68, which is materially similar to claim 23 for purposes of institution. *See id.* at 50–51.

For example, for limitation 23.e, Petitioner contends that "Yusairi discloses generating a packet having *application data* (IP data) and *control bits* (transaction code bits and field type bits) at SOPC Board A." Ex. 1005, 54 § 5.2. Petitioner also contends that "Shin discloses that a packet

(cell) can be formed into codes (input words) that are encoded by block encoding into symbols (code words)." *Id.* (referring to its showing for claim 2). Therefore, Petitioner contends that

> [a] POSITA would have understood that when Yusairi's packet having application data (IP data) and control bits (transaction code and type field) are encoded using Shin's block code, the application data and control bits from the packet (cell) would have been placed into codes (input words) before being encoded into symbols (code words). Ex.1003, ¶189. Thus, by applying Shin's block encoding to Yusairi's packets, the codes (input words) of each packet (cell) would be indicative of application data and control bits. Ex.1003, ¶189.

Pet. 54–55.

Petitioner contends that combining the teachings of Yusairi and Shin would have been obvious because it "would have allowed Yusairi's packet having application data and control bits to be encoded and transmitted as part of a sequence of symbols (code word sequence) using known block encoding methods, such as Shin's 8B/9B block encoding." *Id.* (citing Ex. 1004 ¶ 131; Ex.1003 ¶ 190). Referring to its showing for claim 2 (*id.*), Petitioner contends it would have been obvious to combine the teachings because it "would have provided for flow control at the lower physical and link layers, as opposed to relying on higher-level application functions to provide flow control." *Id.* at 51 (citing Ex.1005, 53 § 4.1 ("For more sophisticated reliabilities or flow control necessary for each application, we rely on functions to be supplied by the application itself."); Ex.1003 ¶ 177; Ex.1009, 129) (discussing link layer functions of prior art systems that performed block encoding and flow control)). Petitioner also contends that the combination "would have provided Yusairi with known communication protocols having a neutral DC component to help ensure [the] signal is

accurately received and decoded by synchronizing the SOPC Board B receiver with the SOPC Board A transmitter." *Id.* (citing Ex.1003 ¶ 177; Ex. 1010, 55) (discussing known prior art systems that used N>M block encoding methods that provided DC balance)).

In response, Patent Owner contends that

> Yusairi explains that the "transaction code" and the "type f[iel]d" values are checked as whole values (0xA and 0x0080 respectively) to confirm the GASP packet meaning that they cannot be divided into individual bits or else they would lose the format confirmation resulting in the IP datagram being either ignored and discarded.

Prelim. Resp. 48. This is similar to Patent Owner's argument discussed in connection with claim 1. Petitioner does not specifically address Patent Owner's argument, as discussed above in connection with claim 1. *See* Reply 4 ("This argument relies on the same incorrect construction and is also tellingly unsupported by its declarant."). Therefore, Petitioner's showing with respect to independent claims 23 and 68 based on Shin and Yusairi is not particularly strong. Additionally, for reasons similar to those discussed above in connection with claims 1, 27, and 68, Petitioner's showing relating to obviousness over Yusairi and Shin for claims 2, 6, 25, 31, 53, 70–72, 74, 75 is not particularly strong.

5. Conclusion Regarding the Merits

The discussion above identifies weaknesses in the Petition that we have considered in our evaluation of *Fintiv* factors. For the reasons given, we determine that this Petition does not present particularly strong merits.

G. Conclusion of Fintiv Factor Balancing

We have considered the circumstances and facts before us in view of the *Fintiv* factors. We take "a holistic view of whether efficiency and

integrity of the system are best served by denying or instituting review" when evaluating these factors. *Fintiv* at 6. Because of the *Sotera* stipulation, factor 4 weighs strongly in favor of not exercising discretion. However, two other factors weigh in favor of exercising discretion, especially the trial date factor. The merits of Petitioner's challenge are not particularly strong. A balanced assessment of the factors leads us to exercise discretion to deny the Petition.

Therefore, we conclude that the evidence of record favors exercising our discretion under 35 U.S.C. § 314(a) to deny institution of an *inter partes* review challenging claims 1, 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, and 75.

IV. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence presented, we exercise our discretion under 35 U.S.C. § 314(a) to deny institution of an *inter partes* review challenging claims 1, 2, 6, 7, 23, 25, 31, 53, 68, 70–72, 74, and 75 of the '307 patent.

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that the Petition is *denied*, and no trial is instituted.

For PETITIONER:

Jason R. Mudd
Lauren E. Douville
Paul M. Vogel
SHOOK, HARDY & BACON L.L.P.
jmudd@shb.com
ldouville@shb.com
pvogel@shb.com

Counsel for Petitioner HP INC.

Brian W. Oaks
Nick Schuneman
Tessa Kroll
MCDERMOTT WILL & EMERY LLP
boaks@mwe.com
nschuneman@mwe.com
tkroll@mwe.com

Counsel for Petitioner DELL INC. and DELL TECHNOLOGIES INC.

Scott Weidenfeller
David A. Garr
COVINGTON & BURLING LLP
sweidenfeller@cov.com
dgarr@cov.com

Counsel for Petitioner LENOVO

For PATENT OWNER:

Brett Cooper
BC Law Group, P.C.
bcooper@bc-lawgroup.com

Robert A. Auchter
AUCHTER PLLC
robert@auchterlaw.com

Seth Lindner
BC LAW GROUP, P.C.
slindner@bc-lawgroup.com