United States Court of Appeals for the Federal Circuit

(Interference No. 105,642)

ELIYAHOU HARARI, ROBERT D. NORMAN, AND SANJAY MEHROTRA,
Appellants

v.

ROGER LEE AND FERNANDO GONZALEZ,
Appellees.

2010-1075

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences.

(Interference No. 105,645)

ELIYAHOU HARARI, ROBERT D. NORMAN, AND SANJAY MEHROTRA,
Appellants,

v.

ANDREI MIHNEA, JEFFREY KESSENICH, AND CHUN CHEN,
Appellees.

2010-1076

Appeal from the United States Patent and Trademark Office, Board of Patent Appeals and Interferences.

Decided: September 1, 2011

WILLIAM A. BIRDWELL, Davis Wright Tremaine, LLP, of Portland, Oregon, argued for appellants. With him on the brief were TIMOTHY R. VOLPERT and SCOTT E. WARNICK.

MEGAN S. WOODWORTH, Dickstein Shapiro LLP, of Washington, DC, argued for appellees. With her on the brief were ERIC OLIVER and THOMAS J. D'AMICO.

Before PROST, MOORE, and O'MALLEY, *Circuit Judges*.

MOORE, *Circuit Judge*.

Eliyahou Harari et al. (Harari) appeals separate decisions of the Board of Patent Appeals and Interferences (Board) in two interferences involving Harari's U.S. Patent Application No. 09/056,398 ('398 application) and several patents assigned to Micron Technology, Inc. (Micron).[1] In the *Lee* interference, the Board entered judgment against Harari on Count 1 of the interference (Harari's corresponding claims are 63-66) on the grounds that there was no written description support for Harari's claims in the specification as filed. Harari argued that it had incorporated by reference its own earlier application,

---

[1] We will refer to appeal 2010-1075 as *Lee*, and appeal 2010-1076 as *Mihnea*.

U.S. Patent Application No. 07/337,579 ('579 application), and that this application provided the necessary written description support. The Board held that the '579 application was not incorporated by reference, and that even if it were, the incorporation was not sufficiently specific in identifying the material Harari needs from the '579 application.

In the *Mihnea* interference, the Board entered judgment against Harari on Count 1 of the interference (Harari's corresponding claims 68, 70, 71, etc.), also on the grounds that there was no written description support for Harari's claims in the specification as filed because the necessary portions of the '579 application were not incorporated by reference. The Board in *Mihnea* also concluded that even if the entire '579 application were incorporated, Micron had shown that some of the claims at issue still lacked written description support.

There was an intervening decision from this court on the incorporation by reference of this patent, *Harari v. Hollmer*, 602 F.3d 1348, 1351 (Fed. Cir. 2010). In light of that decision, and after thorough review of the applications, we conclude that the Board erred in its analysis regarding the incorporation by reference of the '579 application. The Board also erred in its claim construction in *Lee*. Under the proper claim construction, in light of the Board's factual findings, we *affirm* the Board's judgment that Harari's claims in *Lee* lack written description support. In *Mihnea*, however, we *vacate* and *remand* the Board's judgment for determination of unresolved factual issues.

BACKGROUND

Harari's '398 application descends through a chain of continuations and a divisional from U.S. Patent Application No. 07/337,566 (the '566 application). Harari filed

the '398 application as a photocopy of the original '566 application along with a preliminary amendment canceling the '566 application's claims and adding new claims that it stated "are substantial copies" of claims in Lee's U.S. Patent No. 5,619,454 (the Lee patent). *Lee* J.A. 657. Harari later added more claims it asserted "are either exact copies or near exact copies" of claims in Mihnea's U.S. Patent Nos. 6,426,898 and 6,493,280 (the Mihnea patents). *Mihnea* J.A. 917.

On June 23, 2008, the United States Patent and Trademark Office (USPTO) declared Patent Interference No. 105,642 against Lee. *Lee* J.A. 54-55. Several weeks later, the USPTO declared Patent Interference No. 105,645 between Harari and Mihnea. *Mihnea* J.A. 52-53. In both interferences, Micron – the real party in interest representing Lee and Mihnea – filed threshold motions to dismiss, alleging that Harari's involved claims were unpatentable for lack of written description support. Harari asserted that the allegedly incorporated '579 application supported the involved claims. Micron, however, argued that Harari's '398 application failed to incorporate the '579 application by reference.

Micron did not dispute that Harari's original '566 application properly identified the '579 application as "copending U.S. patent application[] . . . entitled 'Multistate EEprom Read and Write Circuits and Techniques,' *filed on the same day as the present application*, by Sanjay Mehrotra and Dr. Eliyahou Harari." *Lee* J.A. 695 (emphasis added). Because the '566 and '579 applications were filed on the same day and were not yet assigned serial numbers, referencing the '579 application by inventorship and title was appropriate.

Micron argued instead that, even though it was a photocopy of the '566 application, Harari's later-filed '398

application failed to identify the '579 application. Micron asserted that the phrase "the same day as the present application" should be interpreted to mean the same day that the '398 application was filed, not the original '566 application's filing date. Both Board panels agreed, and determined that the allegedly incorporated material was instead new matter. Because Harari relied on this material to support the claims at issue, the two Board panels held that Harari's claims lacked written description support.

The Board panels further concluded that even if the '398 application adequately identified the '579 application as the target application, it failed to identify with sufficient specificity the portions of the '579 application relied upon by Harari. The *Mihnea* Board also held that even if the entire '579 application was incorporated, Micron had shown that certain claims, the "offset erase verify bias" claims, still lacked written description support. In contrast, the *Lee* Board concluded that Micron had failed to show that the claims at issue lacked written description support if the entire '579 application was incorporated by reference. The two Board panels thus granted Micron's threshold motions to dismiss and entered judgment on priority against Harari. Harari appeals both cases, and we have jurisdiction under 28 U.S.C. § 1295(a)(4)(A) and 35 U.S.C. § 141.

After the Board panels entered judgment for Micron in the *Lee* and *Mihnea* interferences, we decided *Harari v. Hollmer*, which involved another Harari application similarly descended from the '566 application. 602 F.3d at 1350. Like the '398 application at issue, the Harari application in *Hollmer* was filed as a photocopy of the original '566 application along with a preliminary amendment canceling the photocopied claims, adding new claims, updating the cross-references to related applica-

tions, and inserting text and drawings from the incorporated '579 application. *Id.* at 1350-51. In *Hollmer*, we held that the same incorporation language that is before us in *Lee* and *Mihnea* was sufficient to identify the '579 application. *Id.* at 1351-52. Micron now concedes that, under *Hollmer*, Harari's '398 application adequately identified the '579 application for incorporation. The parties still dispute, however, how much of the '579 application was incorporated.

DISCUSSION

I. Incorporation by Reference

Whether and to what extent a patent application incorporates material by reference is a question of law we review *de novo*. *Hollmer*, 602 F.3d at 1351. In making that determination, the standard is whether one reasonably skilled in the art would understand the application as describing with sufficient particularity the material to be incorporated. *Zenon Envtl., Inc. v. U.S. Filter Corp.*, 506 F.3d 1370, 1378-79 (Fed. Cir. 2007).

Harari argues that in *Hollmer* we held that the entire '579 application was incorporated by reference. We disagree. The parties in *Hollmer* disputed only whether the incorporation language adequately identified the '579 application, and we had no occasion to determine whether all or only some of the application was incorporated. 602 F.3d at 1352 & n.1. Accordingly, *Hollmer* holds only that the photocopied incorporation language is sufficient to identify the '579 application when considered by a "reasonable examiner in light of the documents presented." *Id.* at 1353. *Hollmer* did not address the extent of the incorporation. Because the parties dispute the extent of incorporation, we must now perform that analysis.

The parties' dispute focuses on two passages in the '398 application, i.e., the photocopy of the '566 application. The application first discusses incorporation of the '579 application and another application which is not at issue here:

> Optimized erase implementations have been disclosed in two copending U.S. patent applications. They are copending U.S. patent applications, Serial No. 204,175, filed June 8, 1988, by Dr. Eliyahou Harari and one entitled "Multistate EEprom Read and Write Circuits and Techniques," filed on the same day as the present application, by Sanjay Mehrotra and Dr. Eliyahou Harari. *The disclosures of the two applications are hereby incorporate[d] by reference.* The Flash EEprom cells are erased by applying a pulse of erasing voltage followed by a read to verify if the cells are erased to the "erased" state. If not, further pulsing and verifying are repeated . . . .

Lee J.A. 695 (emphasis added). In a later paragraph, the application again discusses the two applications, but uses different and arguably narrower language:

> Optimized implementations of write operation for Flash EEprom device have been disclosed in two previously cited co-pending U.S. patent applications, Serial No. 204,175, and one entitled "Multi-State EEprom Read and Write Circuits and Techniques." *Relevant portions of the disclosures are hereby incorporated by reference.* Briefly, during the write cycle, the controller applies a pulse of programming (or writing) voltages. This is followed by a verify read to determine if all the bits have been programmed properly. If the bits did

> not verify, the controller repeats the program/verify cycle . . . .

Lee J.A. 706 (emphasis added).

Harari argues that the first incorporation statement plainly and unambiguously incorporates the entire '579 disclosure. According to Harari, the second incorporation statement shows that the inventors knew how to incorporate only a portion of the '579 application and chose not to do so in the first statement. Harari further argues that there is no need to use such words as "in its entirety" to indicate that the entire reference is incorporated. Micron responds that the Board correctly determined that the above-quoted language fails to clearly indicate with detailed particularity that Harari intended to incorporate all of the '579 application. Instead, Micron argues, the incorporation language when read in context indicates that Harari intended to incorporate only the optimized erase and optimized write implementations as described in the short passages following the incorporation language. Micron also argues that the second incorporation statement is superfluous if the first one actually incorporated the entire '579 application.

We agree with Harari that the first incorporation passage incorporates the entire disclosures of the two applications rather than just the portions describing optimized erase implementations. The Board is certainly correct that the incorporation here occurred during a discussion of the erase implementations. We nonetheless conclude that the entire '579 application disclosure was incorporated by the broad and unequivocal language: "The disclosures of the two applications are hereby incorporate[d] by reference." We contrast the incorporation language used here, "the disclosures," with the incorporation language used later in the same specification, "rele-

vant portions of the disclosures." When the drafter intended to incorporate only a portion it did so expressly. While it may seem redundant, nothing prevents a patent drafter from later incorporating again certain "relevant portions" of an application so as to direct the reader to the exact portion of the incorporated document the drafter believes relevant. In the context of this specification and the language used, we conclude that the '398 application incorporates the entire disclosure of the '579 application.

Even if the '398 application was limited to the incorporation of the optimized erase and optimized write implementations of the '579 application, we conclude that all of the sections at issue – the reprogramming feature and the indirect read implementation – are part of the disclosed optimized erase and optimized write. In *Lee*, the Board held that the reprogramming feature was not part of the optimized erase and optimize write implementations. The Board defined the optimized erase and write implementations to include only the erase/verify and the program/verify cycles summarized in brief passages following the incorporation language. The Board reasoned that because "[t]he reprogramming of an erased cell is described in the disclosure of the '579 application as being drawn to a 'different aspect' and 'different feature' of the disclosed invention," the reprogramming feature is "something other than the substantive material properly identified for incorporation by reference." *Lee* J.A. 32-33 (misquoting the '579 application by twice substituting the word "different" for "another").

On appeal, Micron repeats the *Lee* Board's reasoning, and further asserts that reprogramming occurs only after a memory cell has been erased. Harari disagrees, and argues that optimized erase and write necessarily include the reprogramming feature. We agree with Harari. The reprogramming feature is part of the optimized erase and

optimized write implementations described in the '579 application and is therefore incorporated into the '398 application. As a preliminary matter, the fact that the specification refers to the reprogramming as "another aspect" or "another feature" of the present invention is not dispositive of the inquiry. First, we note that the reprogramming discussion cited by the Board appears in the section of the specification entitled: "Read Circuits and Techniques Using Reference Cells." The summary of the invention portion of the patent explains that the invention is "improvements in EEprom array read and write circuits and techniques in order to provide multiple threshold levels that allow accurate reading and writing of more than two distinct states within each memory cell over an extended lifetime of the memory cells, so that more than one bit may be reliably stored in each cell." The reprogramming is part of the read circuits and techniques. As the reprogramming discussion cited by the Board explains, the reprogramming "provides a uniform starting point for subsequent programming of the cells." It makes sure that all of the erased cells are brought to the same state – the ground state. Harari's expert explained that after cells are put into an "erased" state, they are reprogrammed to the ground state to "'provide[] a uniform starting point for subsequent programming of the cells.'" *Lee* J.A. 766 (quoting the '579 application reproduced at *Lee* J.A. 346). As the expert explained, this helps to ensure that the cells undergo the same number of cycles, which helps improve cell accuracy and reliability. *Lee* J.A. 766-67. The expert concluded, "Harari's 'reprogramming' technique completes the erase sequence, in order to initialize all cells to the same 'ground' level *before* data programming commences." *Lee* J.A. 795 (emphasis in original). Therefore, the reprogramming feature is part of the optimized erase implementation disclosed in the

'579 application and therefore was incorporated by reference.

In *Mihnea*, the Board addressed the incorporation of material describing adjusting the bias applied to a reference cell, which is a part of the '579 application's disclosed indirect read implementation. The '579 application describes two read implementations that compare a memory cell value to the threshold values stored in local reference cells. Local reference cells are located in each sector along with the sector's memory cells and store copies of the thresholds stored in master reference cells. Because the local reference cells are subject to the same conditions and number of cycles as their associated memory cells, using local reference cells as a basis for comparison automatically compensates for changes in cell performance over time or due to local conditions. *Lee* J.A. 340, 343-44. The first described read implementation directly compares the memory cell's stored value to a threshold stored in a local reference cell. *Lee* J.A. 342. The second read embodiment indirectly compares the memory cell to the threshold in the local reference cell. The memory cell is compared to the master reference cell's copy of the threshold that has been biased by a value reflecting the local reference cell's copy of the threshold. *Lee* J.A. 343-45. "[E]very time a sector is read, the master reference cells [holding the thresholds] are re-biased relative to the local reference cells, and used for reading the memory cells in the sector." *Lee* J.A. 343-45. Thus, when using this indirect read implementation, "local reference cells (which track threshold deviations of the addressed cells) are used to effectively readjust the breakpoint thresholds of the master reference cells." *Lee* J.A. 343-44.

The *Mihnea* Board determined that the incorporation language failed to sufficiently identify the material re-

garding adjusting the bias applied to a reference cell. *Mihnea* J.A. 35. The Board reasoned that adjusting the bias is part of the indirect read implementation, and that only the direct read implementation is used to verify a cell's status during the erase/verify and program/verify cycles. The Board relied on a portion of the '579 application that states that the "local reference cells are used directly *to read or program/erase verify* the sector's memory cells," while in the indirect read embodiment, "'the local reference cells are used indirectly to *read* the addressed memory cells.'" *Mihnea* J.A. 33-34 (quoting the '579 application as reproduced at *Lee* J.A. 342) (emphases added by Board).

On appeal, Micron repeats the Board's reasoning and further argues that adjusting the bias applied to a master reference cell is performed only to track and compensate for changes to the memory cells over time, and is therefore of little use in the "micro- or nano-seconds between the erasure of the cell and its verification." *Mihnea* Appellee's Br. 38-39. Harari responds that verifying is performed by either of the two read embodiments disclosed in the '579 application.

We again agree with Harari. The '579 application explains that both read embodiments are used to verify. It unambiguously states that local reference cells "are used directly or indirectly to erase verify, program verify or read the sector's addressed memory cells." *Lee* J.A. 342. Furthermore, immediately after describing the indirect read implementation, the '579 application explains that "*the read circuits and operation described are also employed* in the programming and erasing of the memory cells, particularly in the *verifying* part of the operation." *Lee* J.A. 345 (emphases added). The '579 application itself thus expressly states that the described read circuits, the very ones at issue, are part of the verifying process. Even

though Micron argues that adjusting the bias for each read is unnecessary, the '579 application explains that "every time a sector is read, the master reference cells are re-biased relative to the local reference cells." *Lee* J.A. 345. Micron also repeats its arguments from *Lee* regarding the reprogramming feature, which are similarly unavailing in *Mihnea*. Accordingly, we conclude that the material at issue in *Mihnea* was incorporated as part of the described optimized erase and write implementations.

In summary, we conclude that the '579 application was incorporated in its entirety, and that, moreover, the portions of the '579 application that Harari argues provide the written description support for its claims are part of the optimized erase and write implementations.

II. *Harari v. Mihnea*: Written Description

The claims at issue can be divided into two categories: those with an "offset erase verify bias" limitation and those without. In *Mihnea*, the Board held that if the '579 application was incorporated by reference, the claims without an "offset erase verify bias" limitation, such as claim 68, were supported by the specification. On appeal, Micron does not dispute that those claims – those not reciting the offset erase verify bias limitation – are supported if the disputed portions of '579 application were indeed incorporated by reference. With regard to those claims reciting an "offset erase verify bias" limitation, the Board held that they lacked written description support even if all of the '579 application was incorporated by reference. Harari disputes this determination.

Harari's claim 70 illustrates the offset erase verify bias claims at issue here:

> 70. The method of claim 68, wherein said erasing step comprises:

> *offsetting an erase verify bias* used to determine if the flash memory cells are in first of said at least two data states;
>
> applying at least one erase pulse to each flash memory cell;
>
> determining whether contents of the cells are erased using the *offset erase verify bias*; and
>
> repeating said applying and determining steps until all of the cells are erased to a state other than one of at least two data states.

Mihnea J.A. 757, 909-18 (emphases added). The applying, determining, and repeating steps of claim 70 recite an erase/verify cycle at least similar to that described in the '579 application. Memory cells are alternately pulsed with an erase voltage and then verified by comparing to a threshold to see if they are in a non-data state, which Harari's specification calls the "erased" state (which is similar to the "over-erased" condition described in Mihnea). *See Lee* J.A. 345-46; 695-96; Mihnea patent col.6 l.20 - col.7 l.61.[2]

In *Mihnea*, the Board's determination turned on whether the second read implementation could be used to verify the cells. The Board's reasoning echoed its incorporation by reference reasoning: the indirect read – along with its description of adjusting the bias of master reference cells – applied only to the read operation and not the verify operation. *Mihnea* J.A. 36. Thus, the Board concluded, even assuming the indirect read implementation was incorporated, Harari could not rely on it to support the erase verify bias claims. *Mihnea* J.A. 36.

---

[2] All citations to a Mihnea patent specification are to U.S. Patent No. 6,426,898.

We disagree. As we described above with respect to incorporation by reference, the '579 application describes using both the indirect and the direct read implementations to perform the verify portion of the erase/verify and write/verify cycles. The application clearly states that local reference cells "are used directly or indirectly to erase verify, program verify or read the sector's addressed memory cells." *Lee* J.A. 342. Furthermore, immediately after describing the indirect read implementation, the '579 application explains that "the read circuits and operation described are also employed in the programming and erasing of the memory cells, particularly in the verifying part of the operation." *Lee* J.A. 345.

Micron also argues that Harari's offset erase verify bias claims are not supported even if the indirect read may be used to verify. Specifically, Micron argues that Harari's applications never discuss adjusting the threshold of a data state (i.e., offsetting an erase verify bias that is used to determine if a cell is in the data state) to erase a memory cell through the data state into a non-data state as the claims require. Micron asserts that Harari merely adjusts thresholds stored in master reference cells to reflect the values stored in local reference cells. According to Micron, this ensures that cells are erased to the desired state despite memory cell degradation over time. *Mihnea* Appellee's Br. 44. Harari, pointing to the '579 application's discussion of "erase margining schemes," argues that the application describes bias offsets that are used to erase the cell deep into the erased state. *Mihnea* Reply Br. 25.

Mihnea's specification explains that during erase verifying, the memory cell's value is compared to a threshold called an erase verify bias to determine if the cell is in the lowest data state, which it calls the erased state and corresponds to Harari's ground state. By changing that

threshold by some amount, i.e., by offsetting the erase verify bias, the erase/verify cycle will drive the cell's value down until the cell is in a non-data state that Mihnea calls the over-erased state and Harari calls the erased state. In other words, Mihnea applies erase pulses until the cell is verified to be past a new threshold value equal to the erase verify bias including the offset. Mihnea patent col.8 ll.25-50.

In contrast, Harari's '579 application describes an indirect read implementation where the memory cell is compared to a threshold stored in a master reference cell that has been biased by a value reflecting another copy of the same threshold stored in a local reference cell. *Lee* J.A. 343-45 ("[E]very time a sector is read, the master reference cells [holding the thresholds] are re-biased relative to the local reference cells, and used for reading the memory cells in the sector."). Thus, "local reference cells (which track threshold deviations of the addressed cells) are used to effectively readjust the breakpoint thresholds of the master reference cells." *Lee* J.A. 343-44. Because the local reference cells are subject to the same conditions and number of cycles as their associated memory cells, this automatically compensates for changes in cell performance over time or due to local conditions. *Lee* J.A. 343-44.

The '579 application also discusses margining, a procedure that can be used to help compensate for charge retention problems in memory cells. Over time, the stored charge in a memory cell's floating gate may diminish through leakage, which could cause the cell's voltage to drop below a threshold into the next lower state. To compensate, the '579 application discusses putting the memory cell further into the desired state by erasing and programming memory cells past the desired state's threshold by a safety margin. *Lee* J.A. 335, 351-52. For

example, when performing the verification in the erase/verify cycle, a variable voltage is adjusted downward by an amount corresponding to the safety margin, causing the cell to be pulsed further into the desired state. *Lee* J.A. 352.

Thus, the dispute is whether the '579 application's description of margining and biasing a master reference cell relative to a local reference cell provides written description support for the offset erase verify bias claims. We decline to resolve this technical, fact-intensive question in the first instance, and instead vacate and remand to the Board for further proceedings consistent with this opinion.

III. *Harari v. Lee*

In *Lee*, the Board determined that, if all of the '579 application was incorporated by reference, then Micron failed to show that Harari's claims 63-66 lack written description support. Harari's independent claim 63, which Harari asserted is a "substantial cop[y]" of Lee's claim 1, recites:

> A method of *treating* ~~healing~~ at least one ~~over-~~erased *EEprom* ~~memory~~ cell, comprising:
>
> a) accessing a number of control gates and accessing a *bit* ~~digit~~ line, thereby activating *a* ~~said~~ number of memory cells, each of said memory cells having a source, a drain, and a control gate;
>
> b) subsequent to accessing said *bit* ~~digit~~ line, sensing the presence of at least one ~~over-erased~~ activated cell from said number of memory cells *that is erased to a state other than one of at least two data states*; and

> c) subsequent to sensing the presence of said ~~over-~~erased cell, applying a first voltage to said *bit* ~~digit~~ line, a second voltage to said control gate of at least said ~~over~~-erased cell, and a third voltage to said source of at least said ~~over~~-erased cell, said first and second voltages being higher than said third voltage.

Lee J.A. 657, 759; Lee patent claim 1.[3] The Board determined that the broadest reasonable construction of Harari's claim 63 encompassed accessing more than one bit line to activate multiple memory cells. *Lee* J.A. 35-36. The Board reasoned that nothing in the claim language precluded such a meaning, and viewed using a single bit line as a species within the genus of using one or more bit lines. *Lee* J.A. 36-37. The Board concluded that Micron failed to show that Harari's disclosure of accessing multiple bit lines does not provide written description support. *Lee* J.A. 37.

As an alternative ground for affirming, Micron argues on appeal that the Board's claim construction is incorrect, and that under the correct claim construction Harari's claims lack written description support. According to Micron, the plain language of Harari's claim 63 requires that multiple memory cells are activated by accessing their control gates and a single bit line. Harari replies that because "a bit line" means one or more bit lines, the Board's claim construction is correct.

A. Claim Construction

Claim construction is a matter of law we review *de novo*. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1455-56 (Fed. Cir. 1998) (en banc). Because this is an

---

[3] The strikethroughs and underlines reflect Harari's edits to Lee's claim.

interference and Harari substantially copied Lee claim 1, we give the claim its broadest reasonable construction in light of the Lee patent specification. *Agilent Techs., Inc. v. Affymetrix, Inc.*, 567 F.3d 1366, 1375 (Fed. Cir. 2009) (discussing the rule of *In re Spina*, 975 F.2d 854, 856 (Fed. Cir. 1992)). To satisfy the written description requirement, the properly construed claim must be supported by Harari's specification. *Id.* at 1378-79. Micron, as the moving party, bears the burden of proof to demonstrate that Harari's claims as properly construed lack written description support. *See* 37 C.F.R. § 41.121(b). Compliance with the written description requirement is a question of fact that we review under the substantial evidence standard. *Chen v. Bouchard*, 347 F.3d 1299, 1304 (Fed. Cir. 2003).

Harari's arguments rely on our rule that the indefinite article "a" means "'one or more' in open-ended claims containing the transitional phrase 'comprising.'" *Lee* Appellant's Br. 21 (quoting *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008)). In *Baldwin*, we construed a claim reciting a system comprising "a pre-soaked fabric roll" and a "means for locating said fabric roll." 512 F.3d at 1340. We concluded that the claim encompassed systems with more than one fabric roll. *Id.* at 1343.

Baldwin, however, does not set a hard and fast rule that "a" always means one or more than one. Instead, we read the limitation in light of the claim and specification to discern its meaning. *Insituform Techs., Inc. v. Cat Contracting, Inc.*, 99 F.3d 1098, 1105-06 (Fed. Cir. 1996) (analyzing the "claims, specification and file history" to determine that "a vacuum cup" means one and only one vacuum cup). When the claim language and specification indicate that "a" means one and only one, it is appropriate

to construe it as such even in the context of an open-ended "comprising" claim.

In this case, the relevant independent claim does not recite a memory device having "a" bit line. Instead, it recites a *method* comprising accessing a *number* of control gates and *a* bit line to activate a *number* of cells. The plain language of the claim clearly indicates that only a single bit line is used when accessing a number of cells.

As in *Insituform*, nothing in the text of Harari's claim 63 suggests accessing more than one bit line when activating the number of memory cells. For example, step a) expressly distinguishes between the singular and plural by reciting "accessing a number of control gates" while "accessing a bit line" to activate "a number of memory cells." Step b) further reinforces the difference between singular and plural by reciting "subsequent to accessing said bit line, sensing the presence of at least one activated cell." And finally, step c) again distinguishes between singular and plural by applying "a first voltage to said bit line," while applying other voltages to the source and control gate of "at least said erased cell."

We also note that Lee's claim 1 recites "accessing a number of control gates and accessing a digit line, thereby activating *said* number of memory cells." Lee patent, claim 1 (emphasis added). Lee's claim 1 expressly links the number of activated cells to the number of control gates accessed in the row corresponding to the accessed digit[4] line. Therefore, the number of memory cells activated must be the same as the number of control gates accessed. The Lee patent explains that the drains of the cells in one row are all connected to a single digit line. A subset of the cells in the row can be accessed by applying

[4] Lee's digit lines are called bit lines in Harari's '398 application.

a voltage to the control gates of only some of the cells in the row via their control lines, which are connected to the cells in columns. Lee patent col.3 ll.33-40. Lee further explains that if any one or more of the cells in the row are over-erased, the drain voltage (V_D) sensed at that row's digit line will be positive. *Id.* col.3 ll.49-50. If only some of the cells in the row are selected, a positive drain voltage on the digit line reveals if any of the selected cells are over-erased. The Lee patent also discloses, but does not recite in claim 1, finding which cell of the selected cells is over-erased. *Id.* col.3 l.51-64. Lee explains that an over-erased cell can be "healed" by applying a healing voltage for a short time to its drain via the digit line and to its control gate while applying 0 volts to its source. *Id.* col.3 l.65 - col.4 l.18. Lee does not consider accessing more than one digit line at a time but instead describes traversing through memory, digit line by digit line. *Id.* col.3 ll.31-32, col.4 ll.15-20; FIG. 4. The number of cells activated corresponds to the number of control gates accessed. Accordingly, we conclude that the correct and only reasonable construction of the claim terms "a bit line" and "said bit line" as read in light of the Lee specification is that Harari's claim 63 requires that a single bit line activates multiple memory cells.

B. Written Description

This written description decision turned almost entirely on the claim construction. As Micron explains, the '579 application discloses selecting a single memory cell by row and column. In short, there is no disclosure in Harari of a single bit line activating multiple memory cells.

On appeal, Harari argues that the '579 specification describes selecting a plurality of bit lines simultaneously using a drain multiplexer. *Lee* Appellant's Br. 36 (citing

Lee J.A. 330). According to Harari, when multiple bit lines are selected using the drain multiplexer, the bit lines become electrically connected. The Board, however, made a factual determination that the '579 application does not disclose electrically connecting multiple bit lines to form one bit line. *Lee* J.A. 38-39. The Board rejected Harari's argument as unsupported by the testimony of any expert witness. The Board, relying on the testimony of Micron's expert, found that the '579 application does not disclose electrically connecting multiple bit lines to form one bit line. We conclude that this fact finding is supported by substantial evidence.

On appeal, Harari asserts that Micron's expert testimony is "squarely contradicted" by the specification, and thus "is simply not credible on this point." *Lee* Appellant's Br. 37. We disagree. The Board's factual finding is supported by substantial evidence, namely, expert testimony that the '579 application does not disclose or even suggest that a plurality of bit lines can be electrically connected together. *Lee* J.A. 39, 803. Harari points to no section of its disclosure explaining that such selecting electrically connects the bit lines. Moreover, accessing multiple bit lines simultaneously with a multiplexer is not accessing a single bit line. Similarly, calling multiple bit lines a "composite bit line" as Harari does in its briefs does not make it so. Accordingly, we affirm the Board's decision granting Lee's threshold motion alleging unpatentability for lack of written description and its judgment on priority against Harari.

CONCLUSION

For the foregoing reasons, we *vacate* and *remand* *Mihnea* for further proceedings, and *affirm* the Board's judgment in *Lee*.

***Harari v. Lee*, 2010-1075**

AFFIRMED

COSTS

No costs.

***Harari v. Mihnea*, 2010-1076**

VACATED AND REMANDED

COSTS

No costs.