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Paper No. 9
Entered: March 8, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RPX CORPORATION and ADVANCED MICRO DEVICES, INC.,
Petitioner,
v.

IYM TECHNOLOGIES LLC,
Patent Owner.

Case IPR2017-01888
Patent 7,448,012 B1

Before MICHAEL R. ZECHER, MINN CHUNG and
CARL L. SILVERMAN, *Administrative Patent Judges*.

SILVERMAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, RPX Corporation and Advanced Micro Devices, Inc., (collectively "RPX"), filed a Petition requesting an *inter partes* review of claims 1–11, 13, and 14 of U.S. Patent No. 7,448,012 B1 (Ex. 1001, "the '012 patent"). Paper 1 ("Pet."). Patent Owner, IYM Technologies LLC, ("IYM"), filed a Preliminary Response. Paper 8 ("Prelim. Resp.").

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Taking into account the arguments presented in IYM's Preliminary Response, we conclude that the information presented in the Petition establishes that there is a reasonable likelihood that RPX would prevail in challenging claims 1–11, 13, and 14 of the '012 patent as unpatentable under 35 U.S.C. § 103(a). Pursuant to § 314, we hereby institute an *inter partes* review as to these claims of the '012 patent.

A. Related Matters

The '012 patent is involved in a district court case titled *IYM Technologies LLC v. Advanced Micro Devices, Inc.*, 1-16-cv-00649 (D. Del) (the "Delaware Litigation"). Pet. vii; Paper 4, 1. In addition to this Petition, RPX filed a separate petition in Case IPR2017-01886 requesting an *inter partes* review of claims 1–14 of the '012 patent. *Id*.

B. The '012 Patent

The '012 patent, titled "Methods and System for Improving Integrated Circuit Layout," issued November 4, 2008, from U.S. Patent Application No. 10/907,814, filed on April 15, 2005. Ex. 1001, at [54], [45], [21], [22].

The ’012 patent claims priority to the following provisional applications: (1) U.S. Provisional Application No. 60/603,758, filed on August 23, 2004; and (2) U.S. Provisional Application No. 60/564,082, filed on April 21, 2004. *Id.* at [60].

The ’012 patent generally relates to integrated circuit (“IC”) manufacturing and, in particular, to a method and system for generating and optimizing the layout artwork of an IC. Ex. 1001, 1:11–13. As background, the ’012 patent discloses that, in modern processing technology, the manufacturing yield of ICs (i.e., a measure of functioning devices in semiconductor testing) depends heavily on their layout construction. *Id.* at 1:17–19. For a given manufacturing process, a set of design rules are applied during chip layout in order to avoid geometry patterns that cause chip failures. *Id.* at 1:19–21. These design rules guarantee the yield by limiting layout geometry parameters, such as minimum spacing, minimal line width, etc. *Id.* at 1:21–23. Conventional layout construction systems cover the worst case scenario for all chips by applying these design rules over a wide chip area and to entire classes of circuits. *Id.* at 1:24–27.

The ’012 patent discloses that, in modern processing technology, many layout features may interact during chip processing. Ex. 1001, 1:29–31. These feature dependent interactions are difficult to capture with precise design rules and, as a result, sufficiently relaxed global design rules are implemented in order to guarantee the yield. *Id.* at 1:33–36. According to the ’012 patent, there are two drawbacks to this approach: (1) it clearly wastes chip area; and (2) determining the worst case scenario in all chips is a non-trivial task that consumes engineering resources. *Id.* at 1:37–40. The ’012 patent further discloses that some emerging processing technologies

prefer one spatial direction over another. *Id.* at 1:41–42. Existing layout generation systems, however, use identical minimal spacing and minimal width rules for both directions that lead to wasted chip area and underutilization of processing capabilities because the design rules must cover the worst case scenario in both directions. *Id.* at 1:42–46.

The ’012 patent purportedly addresses these and other problems by providing a method and system for forming layout constraints to account for local and orientation processing dependencies. Ex. 1001, 1:51–54. By combining a local process modification value, which represents an additional safeguard beyond an original design rule constraint, with the original design rule constraint itself, it effectively creates a new constraint for every unique local situation. *Id.* at 1:55–64, 4:3–5. This mechanism adds extra safeguards to design rule formulation and improves chip yield by eliminating processing hotspots. *Id.* at 1:64–67, 4:5–6.

C. Challenged Claims

Of the challenged claims, claim 1 is independent and is directed to a method for generating design layout artwork implemented in a computer. Claims 2–11, 13, and 14 directly or indirectly depend from independent claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A method for generating design layout artwork implemented in a computer, comprising:
>
> receiving a design layout comprising a plurality of layout objects residing on a plurality of layers;
>
> receiving descriptions of manufacturing process;
>
> constructing a system of initial constraints among said layout objects;

> computing local process modifications to change said initial constraints using said descriptions of manufacturing process;
>
> constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints;
>
> enforcing said new local constraint distances; and
>
> updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances;
>
> whereby a new layout is produced that has increased yield and performance.

Ex. 1001, 8:16–34.

D. Prior Art References Relied Upon

RPX relies upon the prior art references set forth in the table below:

Non-Patent Literature			**Exhibit No.**
"An Yield Improvement Technique for IC Layout Using Local Design Rules," IEEE Transactions On Computer-Aided Design, Vol. 11, No. 11, Nov. 1992 ("Allan")			1015
Inventor[1]	**U.S. Patent No.**	**Relevant Dates**	**Exhibit No.**
Kroyan	7,523,429 B2	issued Apr. 21, 2009, provisional applications filed Feb. 20, 2004	1006

E. Asserted Grounds of Unpatentability

RPX challenges claims 1–11, 13, and 14 of the '012 patent based on the asserted grounds of unpatentability ("grounds") set forth in the table below. Pet. 7, 20–71.

[1] For clarity and ease of reference, we only list the first named inventor/author.

Reference(s)	Basis	Challenged Claim(s)
Allan (Ex. 1015)	§ 103(a)	1–5, 10, 11, 13, and 14
Allan (Ex. 1015) and Kroyan (Ex. 1006)	§ 103(a)	4 and 6–9

II. ANALYSIS

A. Claim Construction

In an *inter partes* review proceeding, claim terms of an unexpired patent are given their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016) (upholding the use of the broadest reasonable interpretation standard as the claim construction standard to be applied in an *inter partes* review proceeding). Under the broadest reasonable interpretation standard, claim terms are generally given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art, in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In its Petition, RPX proposes constructions for the following claim terms: (1) "width," "space," "overlap," enclosure," and "extension" (claim 13); and (2) "description(s) of manufacturing process" (all challenged claims). Pet. 16–18. In response, IYM does not dispute RPX's proposed constructions for those claim terms. Prelim. Resp. 19. IYM also asserts that RPX does not propose a construction for the claim term "constraints," but nonetheless advocates for a construction of this claim term that is the same

as the construction applied by RPX. *Compare* Prelim. Resp. 16–19, *with* Pet. 33–35.

Because there is no dispute between the parties regarding claim construction, we need not construe explicitly any claim term of the '012 patent at this time. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Obviousness Over the Teachings of Allan

RPX contends that claims 1–5, 10, 11, 13, and 14 of the '012 patent are unpatentable under § 103(a) over the teachings of Allan. Pet. 27–57. RPX explains how Allan teaches or suggests the subject matter of each challenged claim to one of ordinary skill in the art. *Id.* RPX also relies upon the Declaration of Dr. Nagel to support its positions. Ex. 1002 ¶¶ 101–33, 312–414. At this stage of the proceeding, we are persuaded by RPX's explanations and supporting evidence.

We begin our analysis with the principles of law that generally apply to a ground based on obviousness, followed by a brief overview of Allan, and then we address the parties' contentions with respect to the challenged claims.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a

person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;[2] and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).[3] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Allan Overview

Allan "introduces the concept of local design rules" for IC layout optimization at the local level to increase yield. Ex. 1015, 1355. Allan explains that IC layouts are "bound by a set of design rules" that "determine the minimum size and spacing of all layers of the circuit geometry in an attempt to maximize the yield, performance, and reliability." *Id*. Allan explains "the design rules are applied over the whole of the layout area" and are referred to as "global design rules (GDRs)." *Id.* Allan recognizes that these GDRs may give a "good layout . . . but are not necessarily optimized for the local layout conditions." *Id.*

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[2] Relying upon the testimony of Dr. Nagel, RPX offer an assessment as to the level of skill in the art as of April 2004, which is prior to the earliest effective filing date on the face of the '012 patent. Pet. 15 (citing Ex. 1002 ¶¶ 30–32). At this time, IYM does not propose an alternative assessment. To the extent necessary, we accept the assessment offered by RPX as it is consistent with the '012 patent and the asserted prior art.

[3] IYM does not present arguments or evidence of such secondary considerations in its Preliminary Response.

Allan's solution to the non-optimal layout provided by "global" rules is a set of modifications to the global rules, specific to "local layout conditions," which Allan refers to as "local design rules" (LDRs). *Id.* In Figure 1, reproduced below, Allan illustrates an example of its process for increased track widths where permitted by local and global design rules. *Id.* at 1357.

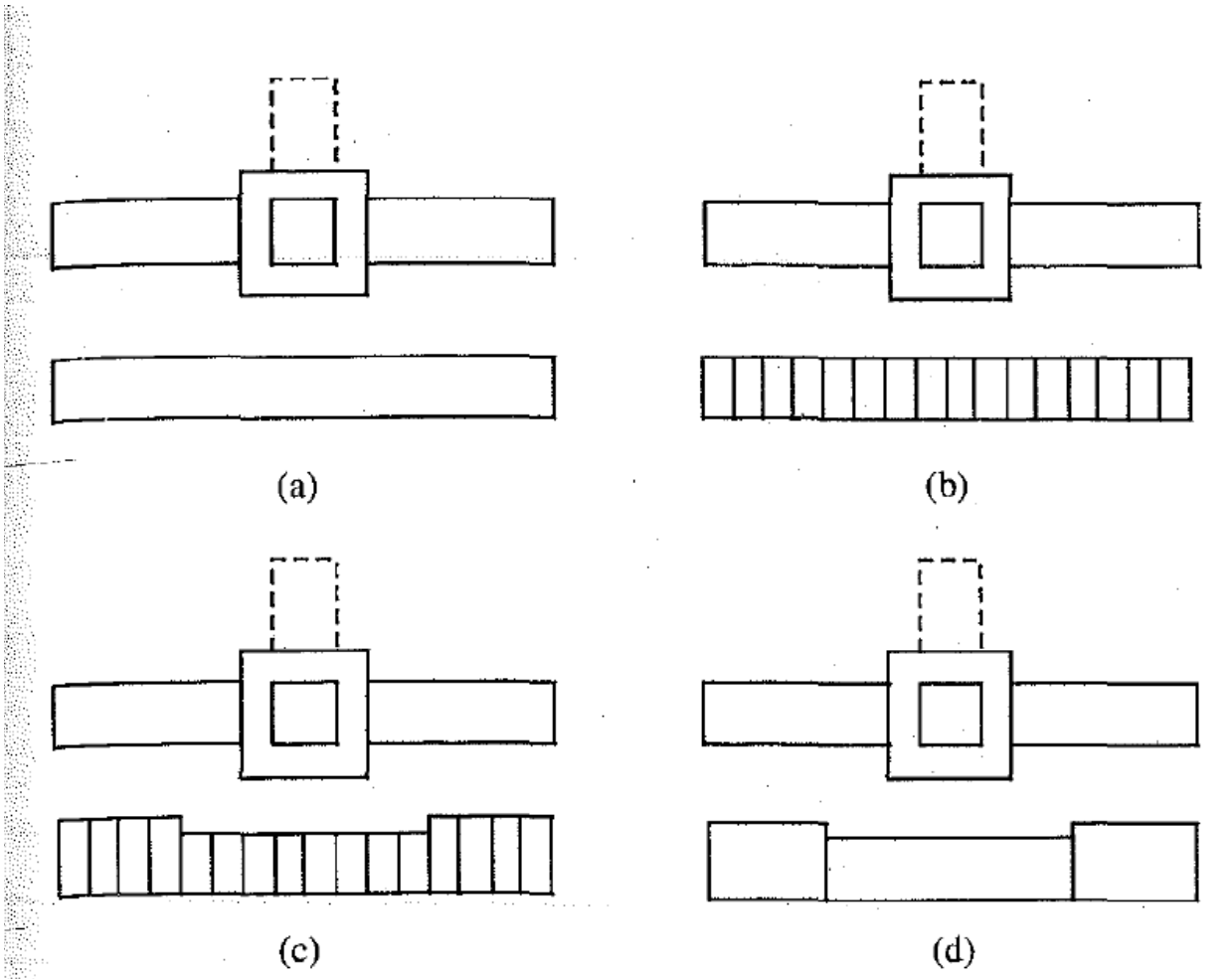


Fig. 1. Application of track width LDR. (a) Original layout. (b) Split track into segments. (c) Increase segment widths where LDR's permit. (d) Merging of segments.

Figure 1(a), reproduced above, describes an "example layout" in which "the bottom metal track has a track width LDR applied to it." *Id.* at 1357. In Figure 1(b), "the track width is split into segments . . . and each segment is tested." *Id.* "If there is space above or below the segment greater than that required for the GDR and the LDR separation, a new wider segment is generated." *Id.* "All the design rules for the new larger segment are checked, and if there are no violations[,] the change in width is accepted," as shown in Figure 1(c). *Id.* In Figure 1(d), the segments are merged. *Id.*

In Figure 2, reproduced below, Allan describes the algorithm used in Figures 1(a)–1(d).

```
Procedure WidthLDR Track
        begin
          Split Track into Segments (see fig. 1(b)).
          for all Segments do {
            if ( Space Above Segment >= LDR + GDR) AND
              ( DesignRuleCheck = OK ) then Increase Segment Size (Top).
            if ( Space Below Segment >= LDR + GDR) AND
              ( DesignRuleCheck = OK ) then Increase Segment Size (Bottom).
          }
          Merge Segments (see fig. 1(d)).
        end
```

Fig. 2. Algorithm for track width LDR.

Figure 2, reproduced above, describes the algorithm used in Figures 1(a)–1(d) wherein the track is split into segments, and for all the segments, if the space above and below the segment is determined to be greater than

LDR + GDR, then the segment size can be increased if the design rule check is OK. Then, the segments are merged.

3. Claim 1

RPX contends Allan teaches all the steps recited in independent claim 1. Pet. 27–47 (citing Ex. 1015; Ex. 1002 ¶¶ 312–378).

Beginning with the preamble "[a] method for generating design layout artwork implemented in a computer," RPX contends Allan describes a computer program ("LocDes") that implements Allan's techniques for analyzing and generating a new layout in which the program acts as a postprocessor of Caltech Intermediate Format (CIF) layout, and "uses the GDR layout to produce an enhanced circuit layout[.]" *Id.* at 28 (citing Ex. 1002, ¶¶ 313–14[4]; Ex. 1015, 1355:§ I, 1356:§ IV). RPX contends Allan's program takes the original layout in CIF format and processes it, using a set of LDR's. *Id.* RPX argues Allan's Figure 9 also shows the program's user interface, which allows the user to apply LDR's to individually selected pieces of circuit geometry. *Id*. (citing Ex. 1015, 1359:§ IV(C)(3), Fig. 9; Ex. 1002 ¶ 314).

RPX contends Allan teaches the step "receiving a design layout comprising a plurality of layout objects residing on a plurality of layers." Pet. 29–31 (citing Ex. 1002 ¶¶ 315–320). RPX argues Allan's CIF layout specification identifies each of the layout's geometric objects, including their coordinates and on what IC layer each object resides. *Id.* at 29 (citing Ex. 1002 ¶ 316; Ex. 1011, 115–27). According to RPX, "[a] POSA would

[4] Although RPX cites Exhibit 1002, ¶¶313–144, based on the context, we understand Petitioner's citation to be to Exhibit 1002, ¶¶ 313–314.

have understood receiving a layout in CIF format would encompass receipt of a layout including multiple objects on multiple layers." *Id.* (citing Ex. 1002 ¶316); *see also* Ex. 1015, 1358–59:§ IV(B).

RPX contends that Allan teaches the step "receiving descriptions of manufacturing process." Pet. 16–18, 31–33 (citing Ex. 1002 ¶¶ 321–28). According to RPX, this term should be assigned its plain and ordinary meaning, and a person of ordinary skill in the art ("POSA") would have understood the plain meaning of this term to be consistent with the later use of this term in claim 1—i.e., "computing local process modifications to change said initial constraints using said descriptions of manufacturing process." *Id.* at 16–17. RPX argues a POSA would have understood that the term encompasses sufficient information to enable "computing local process modifications." *Id.*

RPX contends a POSA would have understood "design rules" and "simulation models" to be examples of information describing a "manufacturing process," and this term ("manufacturing process") would be construed to cover one or both of those, and/or other information. *Id.* at 31. RPX contends Allan describes receiving at least design rules and simulation models. *Id.* (citing Ex. 1002 ¶ 323).

RPX contends defining Allan's GDRs requires knowledge of the process and normally includes the generation of test structures or simulating such test structures. *Id.* at 31 (citing Ex. 1015, 1356:§§ II–II(A)). According to RPX, a POSA would have understood Allan's design rules to be reflective of a manufacturing process. *Id.* at 32 (citing Ex. 1002 ¶ 324). RPX argues Allan notes that deriving LDRs requires even more knowledge of the manufacturing process than GDRs "since the problem is no longer a

'simple' matter of finding one rule set to maximize yield of regular test structures." *Id.* (citing Ex. 1015, 1357:§ II).

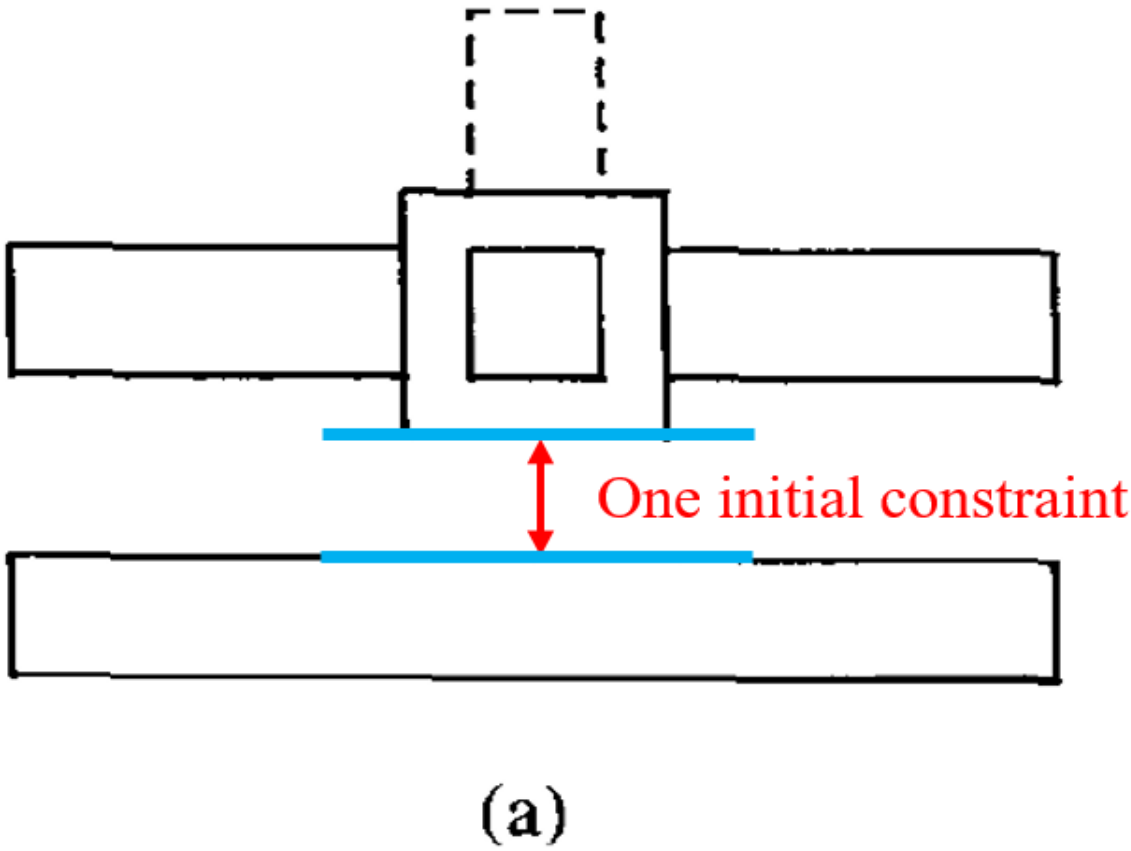
RPX argues Allan teaches the step "constructing a system of initial constraints among said layout objects." Pet. 33–37 (citing Ex. 1002 ¶¶ 329–40).

According to RPX, in the Delaware litigation, IYM argued for a broad construction of "constraints" to mean "limits on geometry parameters of the layout objects in the design layout." *Id.* at 33 (citing Ex. 1017, 4). IYM further indicated that "[o]therwise, no construction [was] necessary." *Id*. According to RPX, because the claim construction standard at the Board is broader than the standard applied in district court, IYM should not be allowed to seek a narrower construction of this term in attempting to distinguish Allan. *Id.* at 33–34 (citing *Rembrandt Wireless Techs., LP v. Samsung Elecs. Co.*, 853 F.3d 1370, 1377 (Fed. Cir. 2017) ("[T]he Board in IPR [*inter partes* review] proceedings operates under a broader claim construction standard than the federal courts.")).

RPX argues the application of design rules (and circuit design considerations) during the design process can determine the "constraints" between adjacent layout objects. *Id*. at 34. RPX argues "[c]onstructing the system of initial constraints," under IYM's construction in the Delaware litigation, is determining the constraints among layout objects in the design. *Id.* (citing Ex. 1015, 3:16–43; Ex. 1017, 4; Ex. 1002 ¶ 331).

RPX contends Allan describes generating a system of constraints arising from application of the GDRs during the design process, which constrains positioning or other dimensions among layout objects. *Id.* at 35. RPX contends Allan describes a set of GDRs, and producing a layout that

has been determined to be compliant with the GDRs. *Id.* (citing Ex. 1015, 1356:§ IV(A)) (disclosing that "the original layout has been passed by a design rule checker"). RPX argues determining whether the original layout is compliant with the design rules involves applying the rules to the layout and creating constraints for each layout object. *Id.* According to RPX, for example, in accordance with Allan's Figure 1, Allan illustrates the result of applying a minimum interobject distance rule between adjacent layout objects, generating a compliant layout. *Id.* Figure 1(a), annotated in red and blue by RPX below, includes at least two layout objects, which for ease of description can be termed the "top" object and the "bottom" object. *Id.* at 35–36 (citing Ex. 1002 ¶¶ 333–34).



In annotated Figure 1(a) above, RPX contends the initial constraint of this example is derived from a GDR regulating an interobject distance, wherein the rule may generally specify that two objects may not be closer than some specified minimum distance. *Id.* at 36. RPX contends the rule becomes a constraint on the two objects shown in Figure 1(a)—i.e., the bottom object must be separated from the top object by at least the minimum distance. *Id.* RPX contends the constraint imposed on the bottom object may be expressed as "Space Above Object >= GDR," where "GDR" is the value of the minimum interobject distance specified by the GDR. Annotated Figure 1(a) above shows the initial constraint in red and the two edges of the two objects driving the positioning of the two objects according to the constraint in blue. *Id.* (citing Ex. 1002 ¶ 334).

RPX argues, because Allan's LocDes program is "a design rule checker" that accepts "only those changes that do not violate any of the global or other local design rules," Allan must have constructed a "system of initial constraints" (under IYM's construction) that captures the constraints between layout objects in the received design layout. *Id.* at 36–37 (citing Ex. 1015, 1356:§ IV, Ex. 1002 ¶¶ 335–36). RPX argues determining this set of initial constraints between layout objects is "constructing a system of initial constraints among said layout objects." *Id.* at 37 (citing Ex. 1002 ¶ 337).

RPX argues Allan teaches the step "computing local process modifications to change said initial constraints using said descriptions of manufacturing process." Pet. 38–40 (Ex. 1002 ¶¶ 341–49). According to RPX, the '012 patent describes that "local process modification to the design rule constraint distance transforms the global design rule constraints into

location specific constraints." *Id.* at 38 (citing Ex. 1001, 3:44–46). RPX contends the '012 patent describes that the "computing" includes *either* performing simulations to derive the modifications *or* retrieving a predetermined value from a look-up table. *Id.* (citing Ex. 1001, 5:1–6:2; *see also* Ex. 1001, claims 8 and 9; Ex. 1002 ¶¶ 342–43).

RPX argues the values specified by Allan's LDRs are the "local process modifications." *Id.* at 38. According to RPX, Allan describes techniques to compute the values for the LDRs, which may be stored for use by its program and Allan also explains that the values of the LDRs are "changes" to the initial constraints. *Id.* (citing Ex. 1015, 1355–56:§ II; Ex. 1002 ¶ 343).

RPX contends Allan describes evaluating a layout using LDRs "to determine where changes in layout generated from GDR set[s] should be performed." *Id.* (citing Ex. 1015, 1355:§ II). RPX argues Allan's LDRs are the "local process modifications," as recited in claim 1. *Id.* RPX argues the LDRs define variations in object dimensions with respect to the original GDRs, based on local conditions within an IC layout. *Id*. According to RPX, Allan specifically observes that "[t]here are a number of potential layout changes that can be made as follows: track displacement, increased contact size . . . , increased contact overlap, increased track width." *Id*. at 38–39 (citing Ex. 1015, 1355:§ I). According to RPX, Allan's LDRs, which are the local process modifications, change the initial constraints (specifying values derived from the global rules) on a layout. *Id.* at 39 (citing Ex. 1002 ¶ 344).

RPX contends Allan's design rules, including its local design rules, are generated using information on a manufacturing process that is to be

used, and are reflective of that manufacturing process. *Id.* (citing Ex. 1015, 1355:§ II.). RPX contends LDRs are applied to GDR-generated layouts to achieve this further local optimization. *Id.* RPX contends Allan further discloses that, "[w]hile it is intended that the yield of the resulting layout will be greater than the initial GDR layout, ***this can be guaranteed only if the fabrication process is understood well enough*** to ensure that the LDRs are an accurate reflection of the relative yield of the layout options under test." *Id.* (citing Ex. 1015, 1355:§ I).

RPX contends the Allan LDRs are computed using the received simulation models. *Id.* at 40. RPX contends the GDRs and the simulation models are a "description of manufacturing processes." *Id.* RPX contends Allan explains that multiple LDRs can be derived from the simulation results. *Id.* (citing Ex. 1015, 1356:§ II(A)). According to RPX, a POSA would have appreciated that, when a tool "applies" an LDR in this manner, the LDR would be predefined, based on the simulations as discussed above, and that the "value" for the LDR would be retrieved from storage. *Id.* at 40 (citing Ex. 1002 ¶ 347). RPX contends retrieving the value for an LDR from a data storage falls within the scope of "computing" a local process modification in this limitation. *Id.* (citing Ex. 1002 ¶ 348).

RPX argues Allan teaches the step "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints." Pet. 40–43 (citing Ex. 1002 ¶¶ 350–61). According to RPX, Allan discloses constructing new local constraint distances by creating new constraints for existing and/or new layout objects, and by combining values specified by LDRs (the local process modifications) with the constraint distances in the initial constraints.

Id. at 40 (citing Ex. 1002 ¶ 351).

RPX argues Allan describes an example of "constructing new local constraint distances." *Id.* at 41. Allan's Figure 1(a), annotated by RPX below, shows the initial constraint.

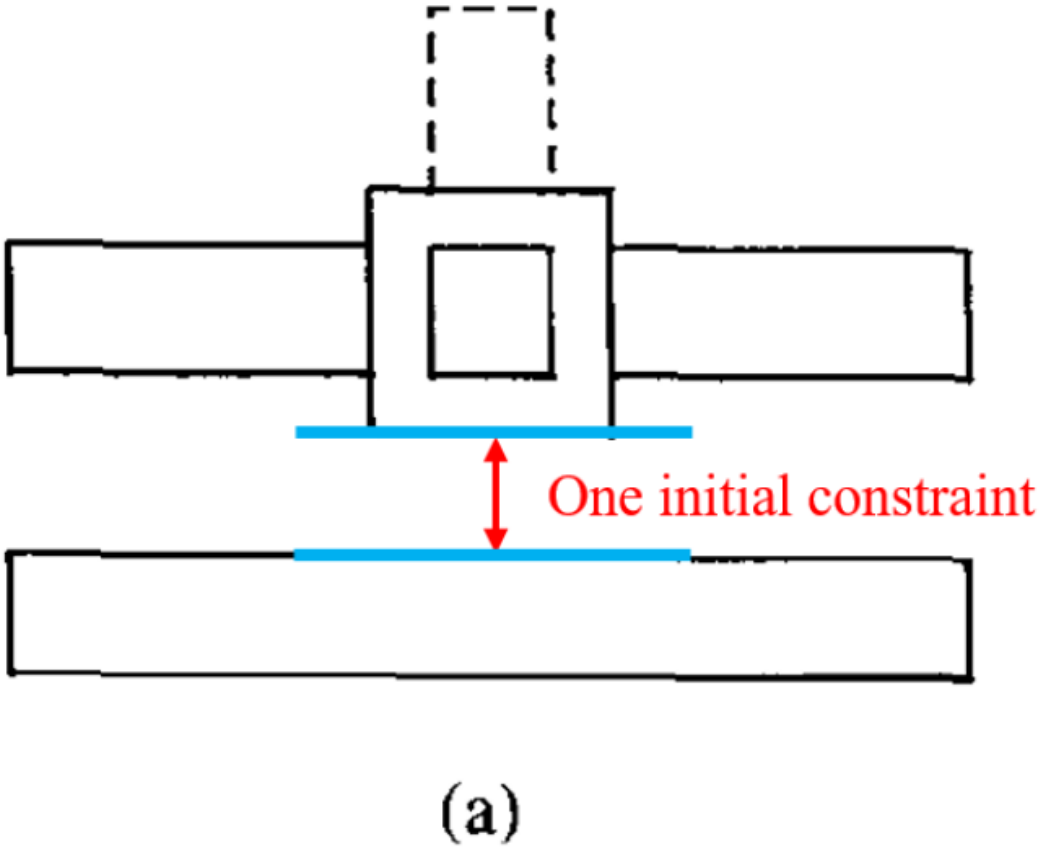


Figure 1(a) annotated by RPX to show one initial constraint

RPX argues Allan's Figure 1(b), annotated by RPX below, illustrates that an original object, to which the single initial constraint was applied, is divided into a set of local objects, such that a local constraint may be identified that is a modification of the single initial constraint. *Id.*

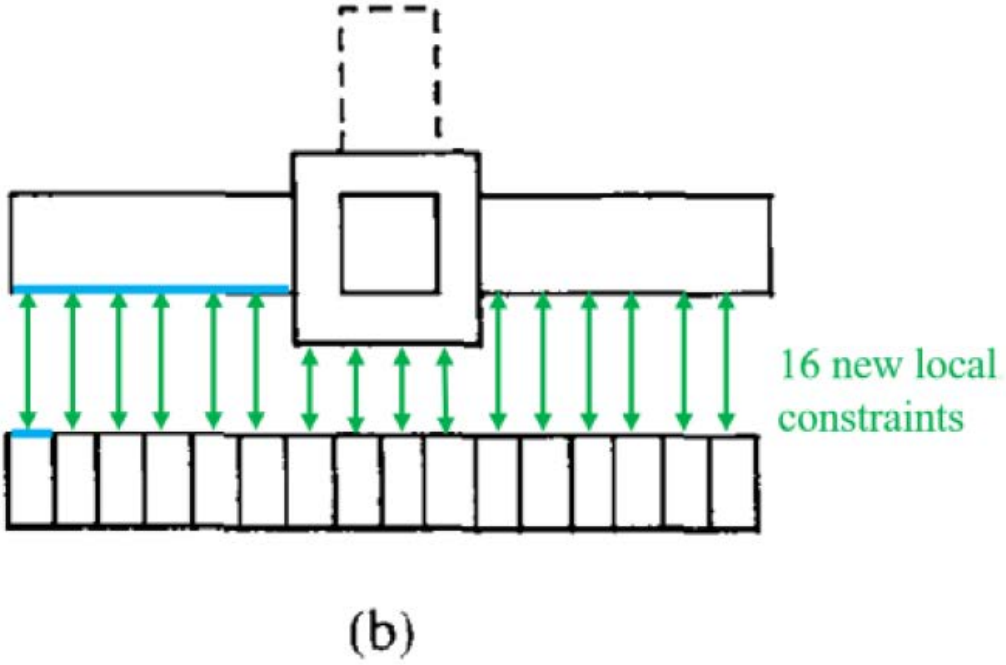


Figure 1(b) annotated by RPX to show 16 new local constraints

RPX argues the new local constraint distances include a constraint distance for each of the new bottom objects (with the existing, top object), where before there was a single constraint, and the new local constraint distances also result from modifying the initial constraint to have a different constraint distance. *Id.* at 41–42. RPX argues Allan describes that a local value for an LDR is added to an initial value from the initial constraint (the GDR) to yield the value for the new local constraint. *Id.* at 42. According to RPX, the new local constraints may even be evaluated using different edges in the layout, as illustrated by comparing the blue lines in annotated Figure 1(b) above. *Id.* (citing Ex. 1002 ¶¶ 352–55).

RPX argues Allan's process leverages the new constraint distances to determine whether and how it can make adjustments to the layout, wherein the new local constraints are evaluated for each local layout object and constrain the ability of Allan's process to make adjustments to the layout in the area of that local layout object. *Id.* (citing Ex. 1015, 1356:§§ I, IV (disclosing that the process "attempts small changes in layout based on the LDR's," accepts "only those changes that do not violate any of the global or other local design rules," and "no changes are made to the layout except where there is good evidence to suggest that a higher yield can be obtained") Ex. 1002 ¶ 356).

RPX argues, in Figure 2, annotated by RPX below, Allan illustrates the new local constraint for each local object, and the process of constructing a new local constraint distance by combining a local process modification with a constraint distance for an initial constraint (*id.*):

if (Space Above Segment >= $LDR + GDR$) **AND**
(DesignRuleCheck = OK) **then** Increase Segment Size (Top).

RPX argues, in annotated Figure 2(a) above, the constraint for each of the multiple "bottom" objects are "Space Above Segment >= LDR + GDR," and the new local constraint is created by combining a local process modification value (specified by an LDR) with the constraint distance specified by the initial constraint (specified by an GDR). *Id.* at 43. RPX argues this new local constraint differs from the initial constraint discussed above regarding Figure 1(a): "Space Above Object >= GDR". *Id.* (citing Ex. 1002 ¶¶ 357–58).

RPX argues each combination of LDR + GDR (i.e., each new local constraint distance) constrains a modification that could be made by Allan's LocDes program. *Id.* According to RPX, in Allan's Figure 2, the combination LDR + GDR constrains whether and how much the track width can be increased by a distance between objects, and therefore creates a "new local constraint distance." *Id.* (citing Ex. 1015, 1357:§ IV(A)(1) ("If there is space above or below the segment greater than that required for the GDR and the LDR separation, a new wider segment is generated. All the design rules for the new larger segment are checked, and if there are no violations, the change in width is accepted (Fig. l(c)).”); Ex. 1002 ¶ 359).

RPX argues Allan teaches the step "enforcing said new local constraint distances." Pet. 43–44 (citing Ex. 1002 ¶¶ 362–65). RPX argues Allan evaluates opportunities for modifying the layout geometry in accordance with the local design rules, so long as such modifications do not violate any of the constraints. *Id.* (citing Ex. 1015, 1356:§ IV (LocDes program "accept[s] only those changes that do not violate ***any*** of the global or other local design rules.").

RPX argues Allan discloses that the algorithm in Figure 2 is "used by the program to ***adjust layout***." *Id.* at 44 (citing Ex. 1015, 1356:§ IV(A), Fig. 2 (showing that the conditional "if (Space Above/Below Segment >= LDR + GDR)" enforces the new constraint by permitting movement up until this condition fails)). RPX argues the "DesignRuleCheck" in combination with "Space Above/Below Segment >= LDR + GDR" enforces the constraints. *Id.* (citing Ex. 1002 ¶ 364).

RPX argues Allan teaches the step "updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances." Pet. 44–45 (citing Ex. 1002 ¶¶ 366–71). RPX contends Allan describes that its program "produce[s] an enhanced circuit layout" and "adjust[s] layout" by using LDRs "to determine where changes in layout … should be performed." *Id.* at 44 (citing Ex. 1015, 1355:§§ I–II, 1356:§ IV(A)). RPX argues, as shown in Figure 2 of Allan and discussed *supra*, if the "if" statement is satisfied, then track width is increased. *Id.* at 45.

if (Space Above Segment $>= LDR + GDR$) **AND**
(DesignRuleCheck = OK) **then** Increase Segment Size (Top).

According to RPX, if these conditions are satisfied, the layout geometry is modified, and then stored in a data structure. *Id.* (citing Ex. 1015, 1358–59:§ IV(B), Fig. 2); *see also* Ex. 1015, Fig. 1, 1357:§ IV(A)(1); Ex. 1002 ¶¶ 368–70.

Finally, RPX argues to the extent that claim 1 "whereby" clause is limiting, Allan discloses "whereby a new layout is produced that has increased yield and performance." Pet. 45–47 (citing Ex. 1002 ¶¶ 372–76).

RPX argues, in the Delaware litigation, IYM contends that the phrase "whereby a new layout is produced that has increased yield and performance" is part of a "whereby" clause "that is not limiting and therefore does not need to be construed." *Id.* at 46 (citing Ex. 1017, 15). RPX argues IYM should not be permitted to take a contrary, narrower position here. *Id.* (citing *Rembrandt*, 853 F.3d at 1377 ("[T]he Board in IPR

proceedings operates under a broader claim construction standard than the federal courts.").

RPX argues Allan is titled "An Yield Improvement Technique for IC Layout Using Local Design Rules," and Allan describes that design rules are used to constrain IC layouts "***in an attempt to maximize the yield, performance***, and reliability." *Id.* (citing Ex. 1015, 1355:§ I). RPX contends Allan further discloses that "***[t]he yield can be increased*** by more effective use of silicon area through the application of local design rules to layouts that have been generated from the normal 'global' design rules." *Id.* (citing Ex. 1015, 1362:§ VI ("Local design rules can be used to ***increase the yield*** in processes that suffer from conductor shorts, contact problems, and conductor breaks[.]")). According to RPX, a POSA would have understood that Allan's techniques are intended to generate a new layout resulting in fabricated integrated circuits with increased yield and performance. *Id.* (citing Ex. 1002, ¶ 374–75).

Based upon our review of the current record, we discern no deficiency in RPX's characterization of Allan and the knowledge in the art, or in RPX's assertions as to the reasonable inferences an ordinary artisan would make from that reference. In addition, for purposes of this Decision, we accept Dr. Nagel's testimony concerning the relevant disclosures of Allan.

In response, IYM argues Allan addresses a fundamentally different problem than the one addressed by the '012 Patent because Allan doesn't disclose the same solution provided by the '012 Patent, RPX blurs anticipation and obviousness, and Allan does not teach five of the seven method steps of independent claim 1. Prelim. Resp. 24–42.

Regarding the fundamentally different problem, IYM contends the '012 Patent is directed to solving a hotspot problem not addressed by Allan, whereas Allan is directed to a very different problem of the best use of any redundant space on an initial layout. *Id.* at 23–24.

On the current record, we are not persuaded by IYM's argument in this regard because claim 1 does not recite hotspots, much less solving a hotspot problem. Ex. 1001, 8:16–34. We note dependent claim 6 recites hotspots (*id*. at 8:48–53); however, RPX's challenge to claim 6 is not based on Allan alone, but instead is based on Allan in combination with Kroyan. Pet. 67–68. In addition, we note that it is well-settled that simply because a reference has a different objective does not preclude a person of ordinary skill in the art from using its teachings in an obviousness evaluation. *See In re Heck*, 699 F.2d 1331, 1333 (Fed. Cir. 1983) ("The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned."); *see also EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985) ("A reference must be considered for everything that it teaches, not simply the described invention or a preferred embodiment.").

We are not persuaded by IYM's argument that RPX blurs anticipation and obviousness. Prelim. Resp. 25–26. Regarding obviousness based on Allan alone, RPX explains:

> The claims call out specific features that do not contribute to the purported inventiveness of the '012 patent and are instead the type of information that publications in this field typically assume is within the reader's knowledge and do not explicitly discuss. For this reason, . . . obviousness grounds are presented rather than anticipation, even where a single reference is cited.

> Dr. Nagel's testimony is cited for these well-known features, together with supporting evidence.
>
> Pet. 8.

Under the circumstances described by RPX, it is appropriate to apply a single prior art reference in light of the common knowledge of one of ordinary skill in the art in analyzing obviousness. *See Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1346–47 (Fed. Cir. 2018) (citing *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016)).

IYM contends Allan does not teach the step "constructing a system of initial constraints among said layout objects" because Allan "says nothing about using constraints," and RPX's arguments and annotations of Allan's' Figures are based on hindsight and attorney arguments. Prelim Resp. 27–34. IYM contends RPX's annotated Fig 1(a) merely represents a distance between two layout objects "without any reference to constraints or minimum spacing requirements or limits." *Id.* at 30. In particular, IYM contends any distance greater than the minimum distance GDR will meet the design rule–"nowhere does Allan disclose that the distance shown in Fig 1(a) is equal to the minimum distance." *Id.* at 30. IYM further contends RPX's one initial constraint in Fig. 1(a) does not appear again and is replaced by four "new local constraint[s]" that are the same as the initial constraint and, therefore, cannot be representing an initial constraint that is subsequently combined with a local process modification to construct local constraint distances. *Id.* at 31–32.

On the current record, we are persuaded by RPX's argument that, when applying the construction of the term "constraints" as "limits on

geometry parameters of the layout objects in the design layout," Allan discloses the initial constraint is the GDR interobject distance. Pet. 36. In particular, the Figure 1(a) bottom object must be separated from the top object by at least the minimum distance and, therefore, "limits geometry parameters of the layout objects in the design layout." *Id.* Regarding the initial constraint of Fig. 1(a), we note this represents the GDR constraint, which is then followed by segmenting and using the LDR. We are not persuaded by IYM arguments to the contrary. Although Allan teaches the claimed constraints, *supra*, we note Allan does not, however, explicitly use the term constraints. It is, however, well established that a reference need not disclose a claim limitation *in haec verba* in order to satisfy that limitation for purposes of anticipation or obviousness. *See Application of Neugebauer*, 330 F.2d 353, 356 n.4 (CCPA 1964) ("In verbis, non verba, sed res et ratio, quaerenda est. (In the construction of words, not the mere words, but the thing and the meaning, are to be inquired after.)").

IYM contends Allan does not disclose the step "computing local process modifications to change said initial constraints" because Allan does not teach "initial constraints," it cannot teach "computing local process modifications to change said initial constraints." Prelim. Resp. 35–37. According to IYM, there is no teaching in Allan of modifying or changing "initial constraints" and IYM argues that RPX engages in impermissible hindsight reconstruction to account for this "computing" step. *Id.* at 45.

On the current record, we are persuaded by RPX's argument that Allan teaches this "computing" step because Allan teaches the initial constraints, *supra*, Allan's' LDRs are computed, constitute the local process modifications, and represent changes to the initial constraints (i.e., GDRs).

Pet. 38–40. Contrary to IYM's assertion that RPX engages in impermissible hindsight reconstruction, RPX's position has a sufficient basis in the teachings of Allan and is supported by the unrefuted testimony of Dr. Nagel. Ex. 1002 ¶¶ 342–348.

IYM contends that Allan does not teach the step "constructing new local constraint distances by combining said local process modifications with constraint distances in said system of initial constraints" because Allan does not teach "initial constraints" and "local process modifications," and therefore it cannot teach this "constructing" step." Prelim. Resp. 37–41. IYM further argues that RPX only asserts that a local constraint may be identified, and that is inadequate. *Id.* at 38.

On the current record, we are persuaded by RPX's arguments that Allan teaches this "constructing" step because it describes combining GDRs (initial constraints) with LDRs (local constraints). Pet. 40–43 (citing Ex. 1002 ¶¶ 350–61). Moreover, we understand RPX's phrase "may be identified" as referring to the inquiry that results in a local constraint.

Lastly, IYM contends that Allan does not teach the steps of "enforcing said new local constraints" and "updating the coordinate variables of layout objects according to the solutions obtained from enforcing said new local constraint distances." Prelim. Resp. 41–42. IYM argues that, because Allan does not teach "new local constraint distances," it cannot teach the "enforcing" and "updating" steps. *Id*

On the current record, we are persuaded by RPX's argument that Allan teaches the "enforcing" and "updating" steps because, as discussed, *supra*, Allan teaches the new local constraints in the form of LDR + GDR. Pet. 43 (citing Ex. 1015, Figs. 1(a), 1(c); Ex. 1002 ¶¶ 357–358). We are not

persuaded by IYM's argument that, because Allan does not teach "new local constraint distances," it cannot teach these "enforcing" and "updating" steps. As discussed *supra*, RPX relies upon Allan's' LDRs as additional constraints to teach the "new local constraint distances." RPX's position has a sufficient basis in the teachings of Allan and is supported by the unrefuted testimony of Dr. Nagel. Ex. 1002 ¶¶ 362–71.

In summary, RPX has demonstrated a reasonable likelihood that they will prevail on their assertion that the subject matter of independent claim 1 would have been obvious over the teachings of Allan.

4. Dependent claims 2–5, 10, 11, 13, and 14

RPX contends Allan teaches the limitations of dependent claims 2–5, 10, 11, 13, and 14. Pet. 47–57 (citing Ex. 1015; Ex. 1002 ¶¶ 379–414). At this stage in the proceeding, IYM does not address separately RPX's explanations and supporting evidence as to how the teachings of Allan account for the limitations of dependent claims 2–5, 10, 11, 13, and 14. *See* generally Prelim. Resp. 23–42. We have reviewed RPX's explanations and supporting evidence regarding these dependent claims, and, on the current record, find them persuasive. *See* Pet. 47–57. RPX, therefore, has demonstrated a reasonable likelihood that it would prevail on its assertion that the subject matter of dependent claims 2–5, 10, 11, 13, and 14 would have been obvious over the teachings of Allan.

C. Obviousness Over the Combined Teachings of Allan and Kroyan

RPX contends that claims 4 and 6–9 of the '012 patent are unpatentable under § 103(a) over the combined teachings of Allan and Kroyan. Pet. 64–71. RPX explains how this proffered combination teaches or suggests the subject matter of each challenged claim, and provide

reasoning as to why one of ordinary skill in the art would have been prompted to modify the references' teachings. *Id.* RPX also relies upon the Declaration of Dr. Laurence W. Nagel, Ph.D., to support its positions. Ex. 1002 ¶¶ 416–61.

At this stage in the proceeding, IYM does not address separately RPX's explanations and supporting evidence as to how the teachings of Allan and Kroyan account for the limitations of dependent claims 4 and 6–9. *See* generally Prelim. Resp. 42. We have reviewed RPX's explanations and supporting evidence regarding these dependent claims, and, on the current record, find them persuasive. *See* Pet. 64–71. RPX, therefore, has demonstrated a reasonable likelihood that it would prevail on its assertion that the subject matter of dependent claims 4 and 6–9 would have been obvious over the teachings of Allan and Kroyan.

D. Constitutional Challenge

IYM contends that we should deny institution because this proceeding violates its right to a jury trial under the Seventh Amendment of the U.S. Constitution. Prelim. Resp. 43. IYM also contends that, because patents are private property rights, disputes concerning their validity must be litigated in an Article III court—not before an executive agency. *Id.* We decline to consider IYM's constitutional challenges because as of this date, the only Article III court to render a decision on the constitutionality of *inter partes* review proceedings has found these proceedings to be constitutional. *See MCM Portfolio LLC v. Hewlett–Packard Co.*, 812 F.3d 1284, 1288–1293 (Fed. Cir. 2015); *cert denied*, 137 S. Ct. 292 (2016). Unless, and until such time as, the U.S. Supreme Court determines that *inter partes* review

proceedings are unconstitutional, we see no reason to consider IYM's constitutional challenges.

Moreover, "administrative agencies [generally] do not have jurisdiction to decide the constitutionality of congressional enactments." *See Riggin v. Office of Senate Fair Employment Practices*, 61 F.3d 1563, 1569 (Fed. Cir. 1995); *see also Harjo v. Pro-Football, Inc.*, 50 USPQ2d 1705, 1710 (TTAB 1999) ("[T]he Board has no authority . . . to declare provisions of the Trademark Act unconstitutional."), *rev'd on other grounds*, 284 F. Supp. 2d 96 (D.D.C. 2003). *But see Am. Express Co. v. Lunenfeld*, Case CBM2014-00050, slip op. at 9–10 (PTAB May 22, 2015) (Paper 51) ("[F]or the reasons articulated in *Patlex* [*Corp. v. Mossinghoff*, 758 F.2d 594 (Fed. Cir. 1985)], we conclude that covered business method patent reviews, like reexamination proceedings, comply with the Seventh Amendment.").

III. CONCLUSION

Taking into account the arguments presented in IYM's Preliminary Response, we conclude that the information presented in the Petition demonstrates that there is a reasonable likelihood that RPX will prevail in challenging claims 1–11, 13, and 14 of the '012 patent as unpatentable under § 103(a). At this stage of the proceeding, we have not made a final determination with respect to the patentability of these challenged claims.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted based on the following grounds:

A. claims 1–5, 10, 11, 13, and 14 as unpatentable under § 103(a) over the teachings of Allan; and

B. claims 4 and 6–9 as unpatentable under § 103(a) over the combined teachings Allan and Kroyan; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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